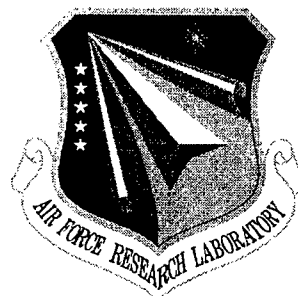


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Final Technical Report

June 2001



MEMS DIRECT VIEW INFRARED VISION SYSTEM (DVIR)

Sarnoff Corporation

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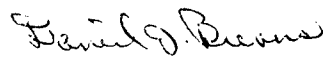
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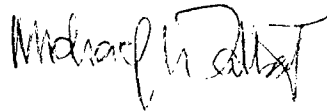
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MEMS DIRECT VIEW INFRARED VISION SYSTEM (DVIR)

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1. Overview

This report summarizes a 2-year research effort by Sarnoff Corporation (Sarnoff) combining MEMS technology with micromachined field emitter technology for the purpose of infrared sensing in the 8-12 μm region. The work was initially funded by Dr. Albert Pisno. After his departure from DARPA, Dr. William Tang was the DARPA program manager. The program monitor was Daniel Burns of AFRL/IFTC. The funding level was \$1,183,679.

1.1 3-Part Objective

The objective of this work was to:

- a. Fabricate 16 x 16 field emitter pixel arrays in which the gates are released with respect to the field emitter tips
- b. Demonstrate field emission current modulation when the gates are activated with IR radiation
- c. Vacuum encapsulate several of these arrays.

1.2 Deliverables

Deliverables include this Final Report and two vacuum encapsulated 16 x 16 arrays that can be activated through IR windows. On 11/13/2000, Sarnoff delivered two units to Daniel Burns of AFRL/IFTC. Figure 1 shows the top and bottom view of one of these units. The top view shows the front of the device containing the CRT phosphor in which the visible IR image appears. The bottom view shows the back of the device containing two ZnSe IR windows and two DVIR chips which contain several fully released 16 x 16 MEMS/field emitter arrays. A stem connector making contact to the emitter substrates, gates, shields, and the front phosphor is shown in the center of the device. Evaporable Ba getters are placed at the periphery and RF activated through

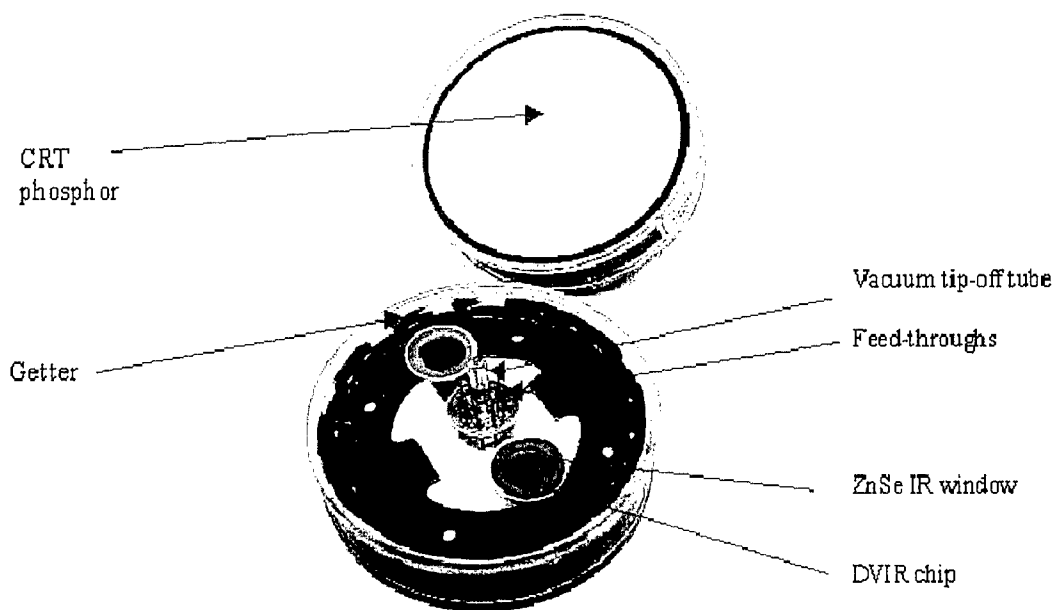


Figure 1. Top and bottom views of two vacuum encapsulated DVIR devices.

the package.

Figure 2 shows the SEM image of one of the pixels and a segment of these pixels within a 16 x 16 array. The pixel contains 30 field emitter tips. The gate plate is connected to an IR absorber plate. Two gold/SiC activators are on either side of the pixel. The absorbed IR energy heats the plate and causes motion of the activators. These in turn move the gate plate which, at a given gate bias, causes modulation of the emission current.

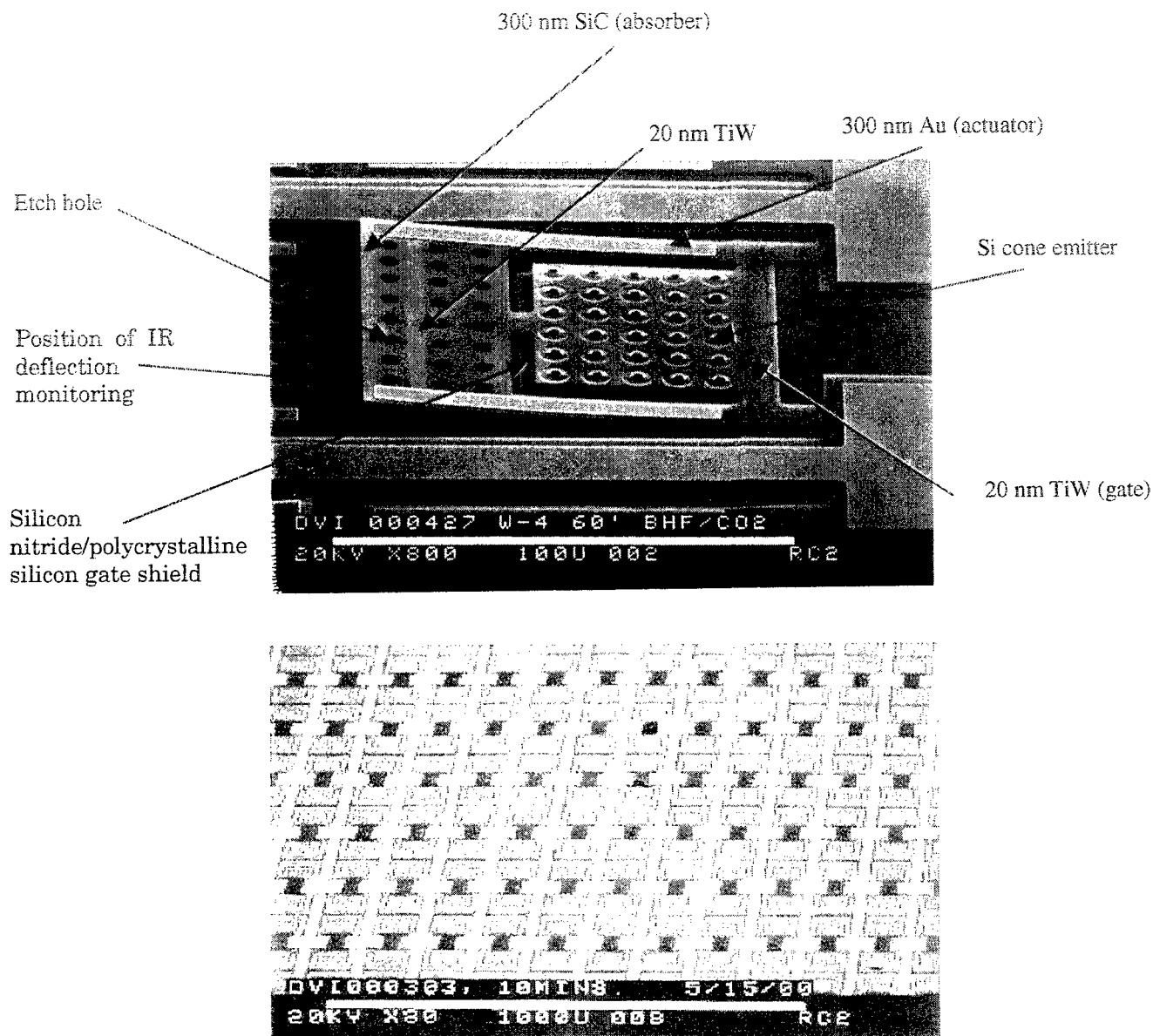


Figure 2. SEM of one pixel element containing 30 field emitter tips (top) and a segment of a 16 x 16 pixel array (bottom).

Figure 3 shows the deflection of the pixel element measured 100 μm away from the anchor as a function of IR power at 10.6 μm . The position where the measurements were taken is marked in Figure 2 (top). The gate plate moves toward the tips with increased IR power, resulting in an increased emission current.

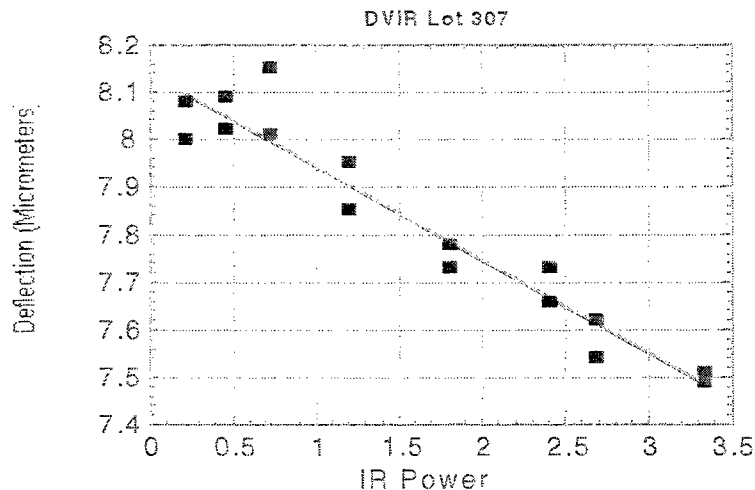


Figure 3. IR deflection of the pixel element in Figure 2. A 10.6 μm laser was used to provide the IR power.

The expected increase in emission current is shown in Figure 4. The Figure shows the calculated emission current for a volcano-shaped gate structure as a function of deflection. Zero deflection means that the apexes of the tips are coplanar with the rim of the gate. Positive deflection means that the rim of the gate is above the tips. The optical profilometer experiments show that the motion of the gate for the device in Figure 2, for maximum and minimum IR powers, is about 0.1 μm for the first row of emitters. That motion corresponds to a 50% increase in emission current according to Figure 4.

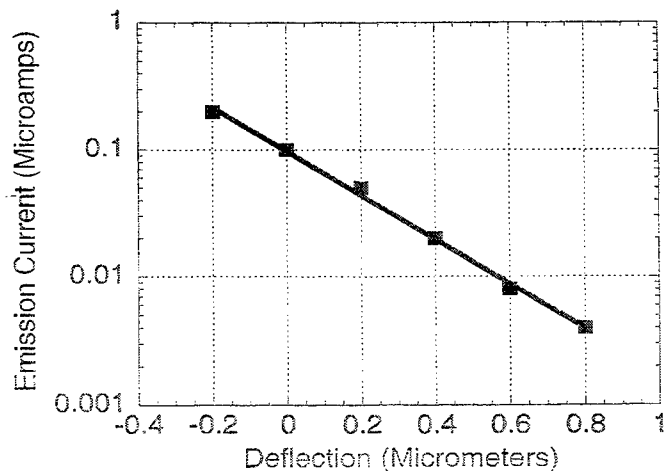


Figure 4. Calculated emission as a function of gate deflection for a volcano-shaped gate structure.

1.3 Accomplishments

1.3.1 Device Fabrication

To meet the objectives, Sarnoff designed and fabricated two sets of devices.

The first set contained individual devices with different gate cantilever lengths, widths, and number of emitters per pixel (ranging from 1-30). Some of the devices contained gate shields. From these lots of devices we obtained a sensitivity of deflection of the 3000 Å Au/3000 Å SiC actuators of $-0.12 \mu\text{m}/^\circ\text{C}/100 \mu\text{m}$. We also performed stress engineering with the end result of near leveraged devices with a 0.85 μm gap and 100 μm long cantilevered gates. We also established the fact that gate shields are necessary. We achieved field emission with turn-on voltages ranging from 50-120 V. But, unfortunately, the devices pulled-in at about 2 V without the shield and 10 V with the shield.

The objectives of the second mask set were to fabricate 16 x 16 pixel arrays, increase the pull-in voltage, and decrease the field emitter turn-on voltage. This was accomplished by fabricating devices with shorter cantilevers (stiffer devices) and smaller gate shield openings near the tips (a reduction from the initial 6 μm to 2 and 4 μm), and by eliminating electrical contact to the IR absorber (reduction of pull-in capacitance). We obtained devices that pulled-in at about 30 V and turned-on at about 80 V. Upon closer inspection of these devices, it was observed that the gate holes, which should have been 2 and 4 μm , were actually 6.7 and 9.7 μm . This was caused by overetching of the polycrystalline Si shield. A final lot was run to correct this problem. But, unfortunately, a mistake was made during the deposition of the sacrificial SiO₂ layer. Instead of SiO₂, Si was deposited and the gates could not be released. At this point, the program was in its concluding phase.

1.3.2 Low Turn-on Voltage Field Emitters

To reduce the turn-on voltage of conical-shaped field emitters, two strategies can be pursued. One is to change their geometry (sharper tips, smaller gate diameters), and the other is to coat the tips with thin layers of appropriate materials. The lowest reported turn-on voltages for Si and Mo tips are about 20 V. These are reported by T. Akinwande [1] and by Candescant [2]. One attempt was made at Sarnoff to fabricate low turn-on voltage tips similar to the MIT tips. The results were not promising and it was decided to pursue the coating strategy. By coating our Si tips with 50 nm of BN or 10 nm of nanocrystalline graphite (NCG), turn-on voltages of 50 V (BN) and of 20 V (NCG) were obtained. Figure 5 shows a representative example of this work.

The effect of the BN and NCG layers is a lowering of the effective work function from about 4.5 eV (Si) to 2.3 eV (BN) and 1.2 eV (NCG).

For DVIR to be a low-cost IR visualization technology, it is desirable to simplify device processing. A breakthrough result (funded partially under this contract and also under the DARPA HERETIC program -- Dr. Elias Towe) was obtained when NCG was deposited into tipless gates. We obtained turn-on voltages as low as 40 V. These are very preliminary results, but they could foster developments with great impact on cold emitter technology. Figure 6 shows the SEM micrograph of one of these 'tipless' devices, its I-V curves and the electron image on a CRT phosphor.

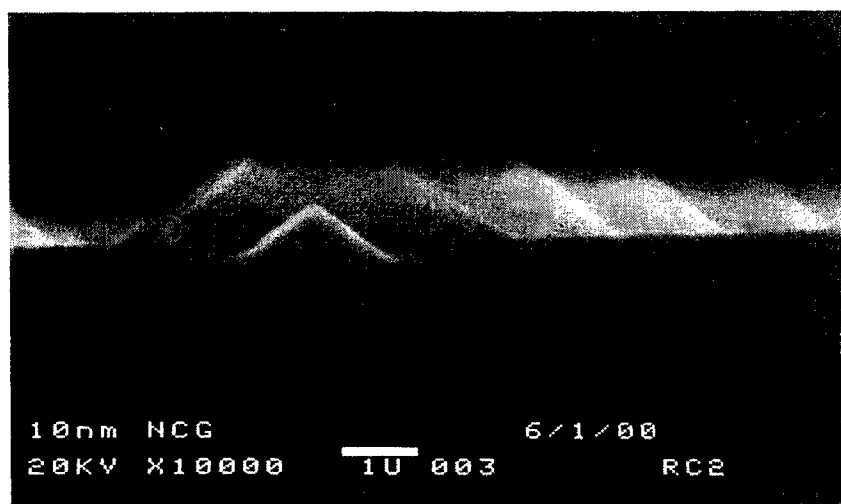
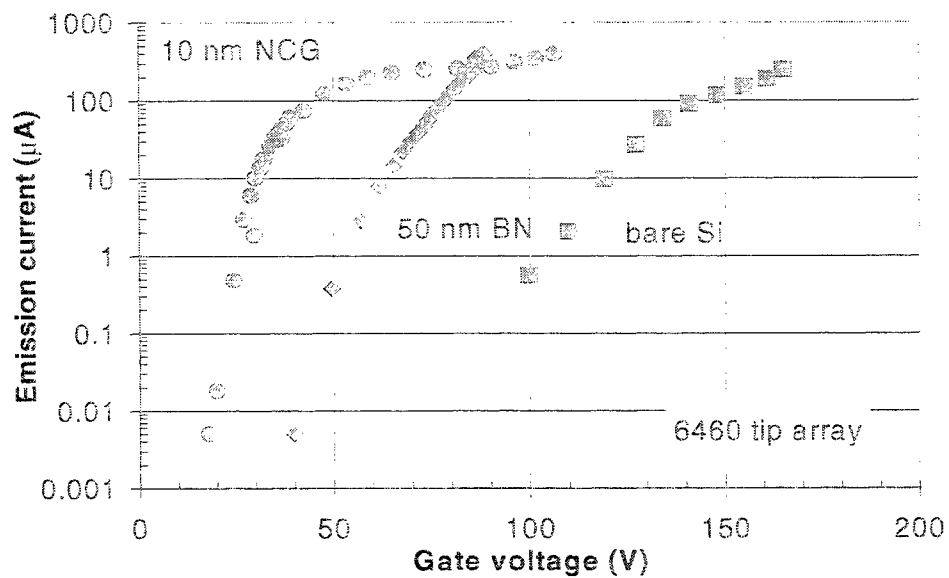


Figure 5. I-V characteristics of a bare Si emitter array and when coated with a 50 nm BN layer and a 10 nm NCG layer. The SEM image shows one of our gated devices coated with 10 nm of BN.

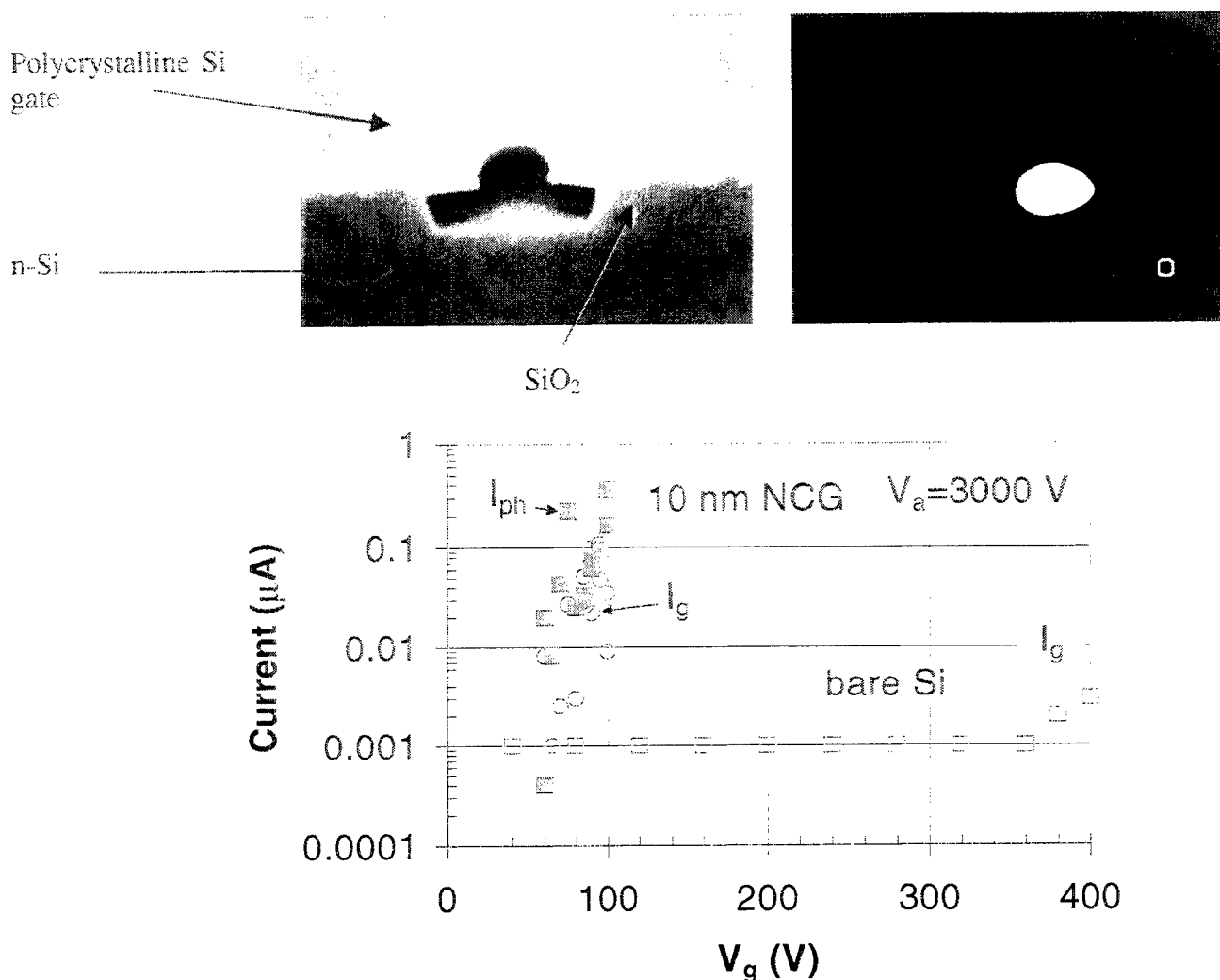


Figure 6. SEM micrograph, I-V curves, and electron beam induced spot on a phosphor screen at a beam current of 0.7 μA and a phosphor voltage of 3000 V. The array contained 6460 holes. The gate diameter is 1.4 μm . This type of emitter structure drastically simplifies the manufacture of DVIR devices.

What cannot be seen from the I-V curves is the fact that Si emitters have to be conditioned. This means that during initial activation, a much higher gate voltage has to be applied to obtain turn-on. Typical examples for our bare Si tip devices are 200-250 V. This means that the devices cannot pull-in prior to reaching these initial high voltages. Fortunately, the NCG and BN coated devices do not need this conditioning. We believe that the native silicon oxide has to be altered by creating defect states, or be removed via electrodesorption in order for the tips to turn on at lower voltages. NCG and BN do not have a native oxide that must be conditioned. To reduce the native oxide of Si tip devices, we installed a DC hydrogen plasma system. Some reduction in turn-on voltages was achieved, but this approach was not very reproducible and needs significant refinement in terms of choosing the appropriate plasma power, temperature, and hydrogen pressure.

1.3.3 Shield Technology

Figure 7 shows the cross-section of a DVIR device with a silicon nitride/n-doped polycrystalline silicon gate shield. By applying the gate voltage also to the shield, a field-free region is obtained except in the vicinity near the tips. To investigate the effect of that region upon the pull-in voltage, devices with 2 μm and 4 μm shield openings have been designed. Unfortunately, during processing, the polycrystalline silicon layer was overetched, resulting in a larger unprotected area than anticipated.

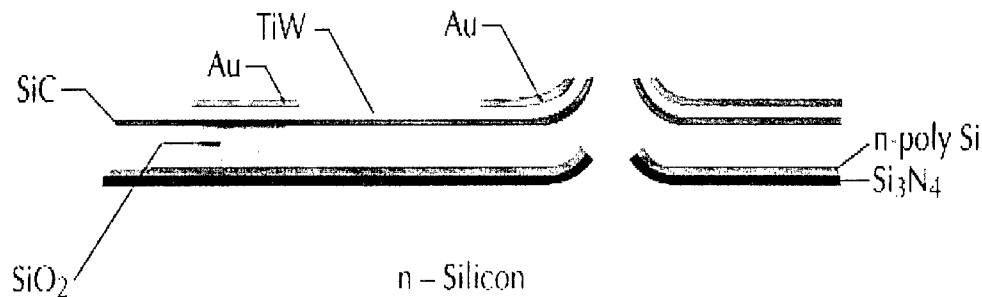


Figure 7. Cross-section of a DVIR device with a gate shield. By applying the gate voltage also to the polycrystalline silicon layer of the shield, a field-free region is obtained except in the vicinity near the tip. The substrate containing the tip is at ground potential.

Figure 8 shows the pull-in results of two devices similar to the one in Figure 2 when the shield is at ground potential (low pull-in voltage) and when it is properly biased with the gate potential. Figure 9 shows the corresponding overetched polycrystalline silicon shields. The underlying insulating silicon nitride layer has been etched correctly.

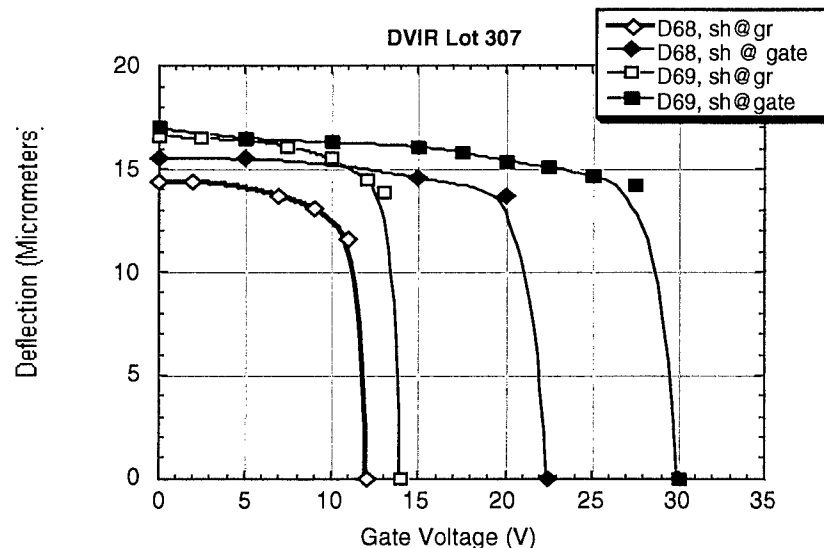


Figure 8. Pull-in voltages for devices in Figure 2 with intended 2 μm (D69) and 4 μm (D68) diameter shield openings. Due to incorrect processing, the shield openings are 6.7 μm and 9.7 μm , respectively. The low pull-in voltage results are obtained by biasing the shield to ground potential.

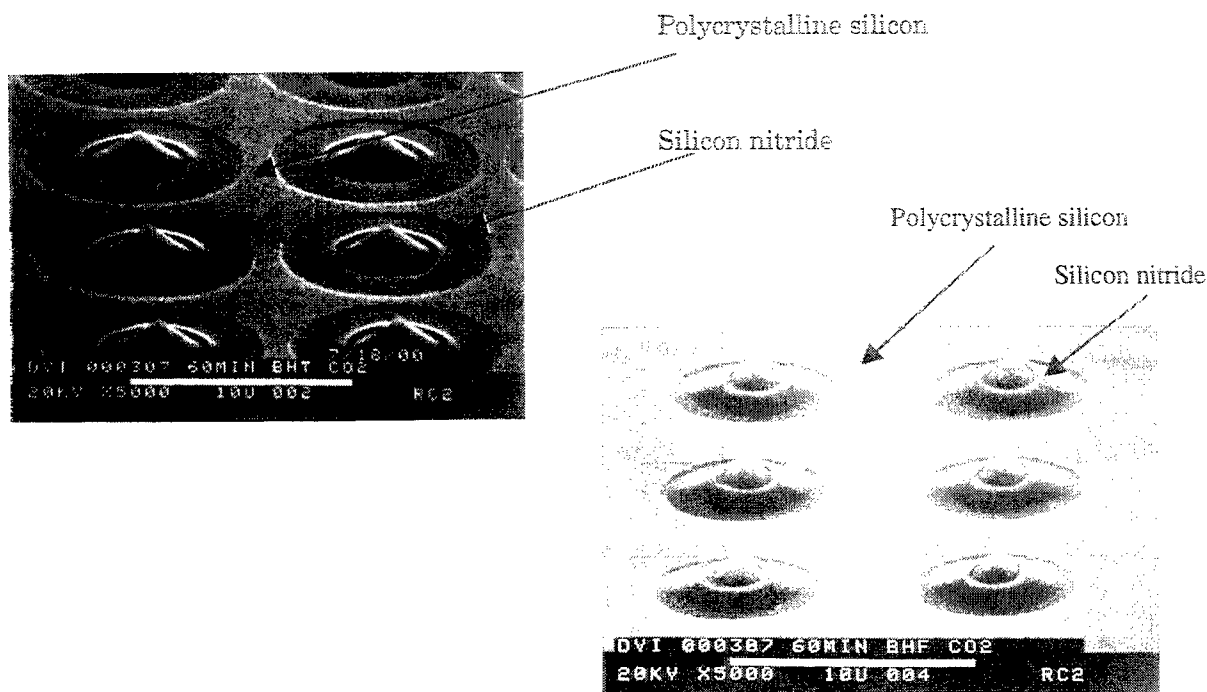


Figure 9. SEM micrographs of overetched 4 μm and 2 μm shield structures. The actual values of the polycrystalline silicon openings are 9.7 μm and 6.7 μm . The diameters of the silicon nitride are 4.5 and 2.1 μm , which are close to the design value of 4 and 2 μm .

We investigated two shield doping levels:

- Heavily doped shield using POCl_3 (875° C anneal, sheet resistance 40 Ω/\square)
- Lightly doped shield using phosphorus ion implantation (50 keV, $2 \times 10^{14} \text{ cm}^{-2}$, 800 °C activation for 2 hours in N_2 , sheet resistance 3000 Ω/\square).

All of the devices fabricated with the first mask set had the heavily doped shields. Experimentally, it was determined that this shield does not transmit IR. About 85% of the incident IR power is reflected, and 15% is absorbed. Based on that information, most of the shields for the arrays in the second mask set are only fabricated within the emitter array. The IR absorber and activator are electrically decoupled from the gate contact and thus do not pull-in when a gate voltage is applied. The device in Figure 2 is of that construction.

By reducing the doping level of the polycrystalline silicon via ion implantation, a shield was developed that is IR transparent. This fact was not known when we designed the second mask set.

1.3.4 Vacuum Encapsulation

For Si field emitters to operate properly, devices have to be encapsulated at pressures below 1×10^{-7} Torr. Encapsulation is not a simple task, since the emitters are very sensitive to monolayer thickness changes of their surface chemistry. Standard CRT techniques of frit sealing in air are

not acceptable for field emitter displays since they cause large increases in turn-on voltages. As an initial attempt in vacuum sealing DVIR devices, we chose the following path:

- Use high temperature frit sealing to bond the phosphor plate to the spacer ring and the stem and feed through pin to the bottom plate
- Connect the ceramic plate to the bottom plate using conductive epoxy
- Bond the DVIR chip to the ceramic substrate using polyimide/silver paste and make the appropriate gold wire connections between gates and shields to the ceramic substrate by also using the polyimide/silver paste
- Use low temperature Torr seal to bond the IR ZnSe windows to the bottom plate and the bottom plate to the spacer ring. This process was chosen to avoid pull-in of the gates during a potential 450 °C frit sealing procedure
- Evacuate the unit through the stem, pinch-off the stem and activate the getters.

Figure 10 shows the cross-section of an encapsulated DVIR device and Figure 1 shows the actual prototype.

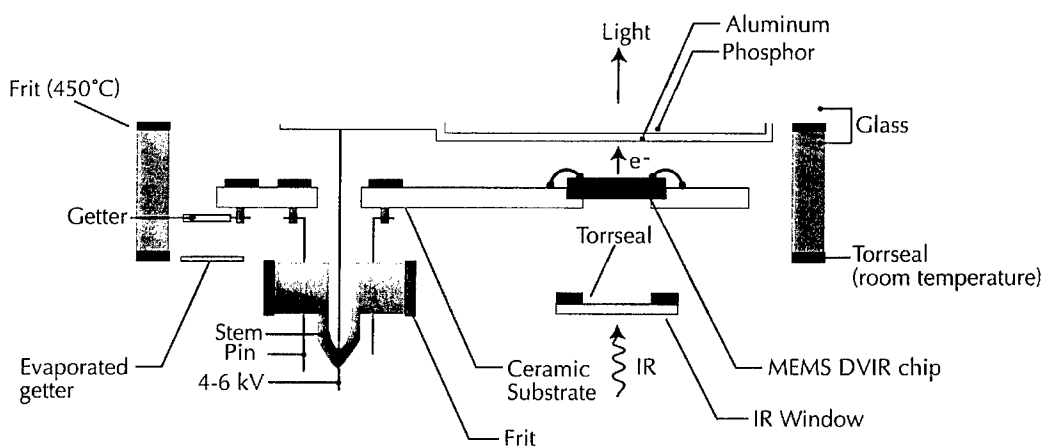


Figure 10. Encapsulation scheme for a prototype DVIR device.

1.3.5 Shortcomings Against Objectives

We have demonstrated all aspects of the proposed work, which include fabrication of fully released 16 x 16 arrays, modulation of the arrays with IR power, and field emission of partially released structures. Due to a processing error, the shield structure was not optimized (overetching of the holes near the tips) and pull-in occurred at about 30-60 V, prior to field emission. The processing error was corrected in one last attempt near the end of the program but, unfortunately, the SiO₂ sacrificial layer was deposited with excess silicon due to malfunctioning of a mass flowmeter and could not be properly removed in buffered HF. Thus, direct modulation of the emission current with incoming IR was not demonstrated.

We did not spend much time on developing an appropriate absorption layer. We relied on the weak absorption properties of SiC to demonstrate modulation and obtained a sensitivity of about -0.34 $\mu\text{m}/\text{W}/100 \mu\text{m}$. The IR power in W is the power of the beam as it enters the DVIR chip from the back of the chip. About 50% of the power is reflected/absorbed by the chip.

We identified a poly ethylene glycol (PEG)-like coating as a potential IR absorber and demonstrated that it can be patterned over selective areas by photoresist lift-off. This work was performed in collaboration with Dr. Y. Vickie Pan of the University of Washington, Seattle, WA. We also demonstrated that 100 nm of sputtered BN is a very effective absorber, but did not pursue this fact any further.

Table 1 summarizes the progress of this work.

Table 1. Progress Summary.

Achieved	Not Achieved
<ul style="list-style-type: none"> Fabricated fully released 16 x 16 arrays. Demonstrated actuator thermal sensitivity of -0.12 $\mu\text{m}/^{\circ}\text{C}/100 \mu\text{m}$. Demonstrated IR motion of pixel of -0.34 $\mu\text{m}/\text{W}/100 \mu\text{m}$ at 10.6 μm IR with 300 nm of SiC as the absorber. Developed a silicon nitride/polycrystalline silicon gate shield technology that is transparent to IR. Identified poly ethylene glycol-like film and BN as potential thin film absorber materials. Obtained 30-60 V pull-in of pixels with non-optimized shields. Obtained turn-on voltages of Si cone emitters ranging from 20-50 V when coated with NCG or BN. Non-coated devices turn on at about 80-100 V, but have to be conditioned at about 200-250 V. 	<ul style="list-style-type: none"> Integration of low turn-on voltage coatings with fully released pixels. Demonstration of IR induced modulation of emission current. Improved IR sensitivity with thin film absorber coating. Field emission in vacuum encapsulated prototype.

1.3.6 Proposed Solutions

Shield process – The shield process has to be optimized. The smallest shield diameter for which data were taken is 6.7 μm . It should have been 2 μm . A final lot was processed with corrected shields, but the cantilevered gates could not be released due to an error in the sacrificial layer deposition. Theoretical modeling of the structures, based on initial experimental results has to be preformed.

Reduced turn-on voltages – Quite a bit of effort was expended integrating the low turn-on voltage coatings into the process. When partially released devices were coated with BN, we obtained turn-on voltages of about 40 V. However, when these devices were then release etched in buffered HF, the turn-on voltage shifted to about 60 V. It might be possible to restore the initial turn-on voltage with a low temperature anneal. However, the annealing procedure has to be chosen so that the gates do not stick after the process. (The gates move towards the substrate when heated). Similar results were obtained with NCG and more work is needed to refine the process.

Split-gate approach – A novel solution to the high turn-on voltage problem was proposed by Dr. Jia Ming Chen of Sarnoff. It consists of splitting the gate into two sections. One of the sections stays anchored after release etching and the other one, connected to the absorber and IR actuator, is released. The anchored section can then be used to condition the tips without pull-in taking place. After conditioning, the anchored section can be biased close to device turn-on, and the released section is biased below the pull-in voltage. The principle of field superposition of the split gate has been demonstrated in [3]. Figure 11 shows the top view of a gate using the split gate approach.

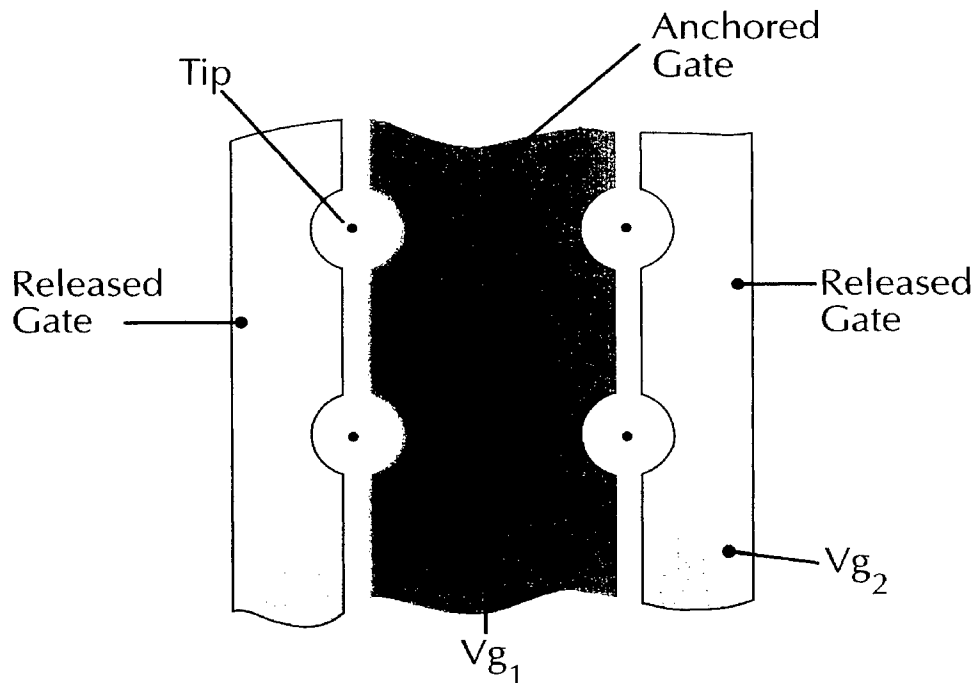


Figure 11. Top view of a split gate.

1.3.7 Impact to DOD

If properly developed, MEMS DVIR offers a low cost, potentially high sensitivity direct view uncooled IR imaging system. Due to the statistical nature of the emission sites, DVIR will not compete with cooled, low noise IR technology but should find a niche for surveillance applications, rescue missions in smoky environments, etc.

The SiC-TiW/Au cantilever technology yields almost stress-free devices. We demonstrated 0.7 μm intrinsic stress-induced deflection of a 100 μm long cantilever.

The shield technology that has been developed can be applied for other MEMS-based products, in which sensory read out requires biasing the moving segments of the device with respect to the stationary segment. In addition to DVIR, an example might be a MEMS gyroscope using nanometer tunneling or field emitters for deflection monitoring.

Cantilever arrays are currently being considered for bioMEMS such as DNA analysis [4]. IR-activated cantilever arrays offer remote activation and do not have to rely on on-board heaters,

which are hard to hermetically seal in a wet environment. By using IR reflective and IR transmissive shields, predetermined patterns of activation can be fabricated into the array. The cantilevers can also be used for egg or cell manipulation, such as piercing a cell with a hollow needle and subsequent injection of bioengineered DNA material.

1.3.8 Publications and Patents

Several publications and one issued patent resulted from this work. One patent disclosure on the split-gate approach was filed with the Sarnoff patent office.

U.S Patent No.: 6,140,646, "Direct View Infrared MEMS Structure", H. H. Busta, R. Amantea, issued on 10/31/2000.

- a. H. Busta, D. Furst, R. Pryor, Lihua Li, "Performance improvement of gated silicon field emitters with a thin layer of boron nitride," Technical Digest, International Vacuum Microelectronics Conference (IVMC) 2000, Guangzhou, China, (2000). Paper submitted to J. Vac. Science Techn. B.
- b. H. Busta, R. Amantea, D. Furst, C. Ling, L. White, and J. M. Chen, "MEMS direct view infrared vision system (DVIR) with FED readout," Technical Digest, IVMC 2000, Guangzhou, China, 232, (2000).
- c. H. H. Busta, D. A. Furst, A.T. Rakhimov, V. A. Samorodov, V. B. Seleznev, and N.V. Suetin, "Reduced turn-on voltage of silicon field emitter array coated with a 10 nm layer of nanocrystalline graphite," unpublished.
- d. H. H. Busta, D. A. Furst, A. T. Rakhimov, V. A. Samorodov, V. B. Seleznev, N. V. Suetin, and A. Silzars, "Low voltage electron emission from 'tipless' field emitter array," paper submitted to Applied Physics Letters, Dec. 2000.
- e. I. Jafri, H. Busta, S. Walsh, "Critical point drying and cleaning for MEMS technology," Proceedings of SPIE, MEMS Reliability for Critical and Space Applications, Vol. 3880, 51 (1999).

2. Introduction

This report describes a 2-year research effort developing an uncooled IR sensing technology that utilizes MEMS cantilever technology with a field emitter readout scheme. MEMS cantilever technology for IR sensing has been described in [5], and implementations using capacitive and optical readout schemes to monitor the MEMS plate deflections have been reported in [6] and [7-9], respectively. Both of these readout schemes are passive, meaning there is no intrinsic gain in the MEMS structure. By using arrays of field emitters in which the MEMS activated gates move relative to the apexes of the tips, a mechanical amplifier of high sensitivity can be constructed. The high sensitivity arises from the fact that the emission current varies exponentially with the electric field at the tips.

The objective of this research was to demonstrate modulation of 16 x 16 pixel arrays as a function of IR modulation in the 8-12 μm wavelength range. The key milestones were to demonstrate IR activation of individual pixel devices by September 1999, and demonstrate proof-of-concept of a vacuum encapsulated 16 x 16 pixel array by September 2000.

Logistically we approached this work by first fabricating SiC/Cr based actuators. The reason for Cr was its resistance towards buffered HF when the sacrificial SiO_2 layer was removed. The choice of SiC as the thermally insulating material was an outgrowth of the DARPA-funded uncooled IR work (COQUI) at Sarnoff. Sarnoff demonstrated that hydrogenated amorphous SiC has superior thermal isolation properties over silicon nitride. We found that under thermal activation, the cantilevers moved in the wrong direction due to a close match of the thermal coefficients of expansion of the two materials. The sensitivity was 0.01 $\mu\text{m}/^\circ\text{C}/50 \mu\text{m}$ long cantilever, which is very low. Aluminum would be the best material in terms of maximum sensitivity, but it is readily attacked during release etching. We then compromised in using gold and needed to install dedicated work areas in the Sarnoff IC facility to avoid possible contamination with other processes. (Gold is a lifetime killer for silicon devices.) Subsequent cantilevers were fabricated in SiC/Au, with a thin (20 nm) thick layer of TiW serving as a conductive layer to the gates in regions where Au had to be omitted for thermal isolation reasons. After fabricating individual devices and establishing the fact that pull-in occurred at relatively low voltages, we designed 16 x 16 arrays with stiffer cantilevers and improved shields. After solving some of the processing issues related to the overetching of gate shield holes, a final lot was processed that should have enabled us to demonstrate the concept. Unfortunately, the final lot resulted in non-functional devices due to a malfunction of a mass flow meter. Instead of SiO_2 , a very silicon rich layer was deposited that could not be removed in buffered HF.

In addition to fabrication and IR testing, quite a bit of effort was expended in vacuum encapsulation. From field emitter display work, we knew that every step in packaging, such as bonding the chips to a substrate using silver epoxy, can affect field emitter turn-on voltages. We systematically simulated every step of the packaging process and measured the performance of the filed emitter arrays after each step. A total of four vacuum packages were produced. Vacuum packaging was performed by Thomas Electronics in Wayne, NJ. Over the years, we worked successfully with Thomas Electronics on field emitter encapsulation issues.

3. Methods, Assumptions, and Procedures

3.1 Principle of Operation

The basic principle of DVIR is shown in Figure 12. It depicts two gated silicon field emitter tips. On the left, the gate is at a higher position as compared to the gate on the right. The motion of the gate is caused by an IR activated cantilever to which the gate is connected. By applying a gate voltage with respect to the tip, the emission current of the left device at temperature T_1 is less than the emission current of the right device at $T_2 > T_1$.

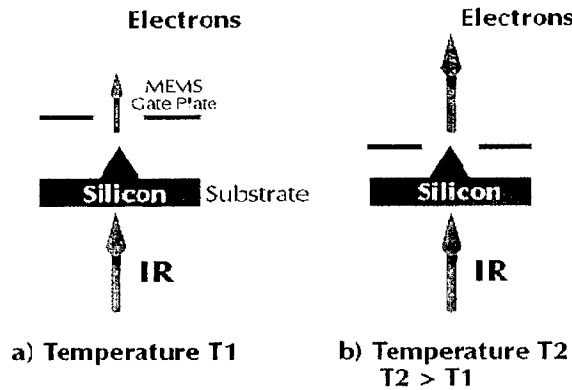


Figure 12. Concept of temperature activated gate motion.

The conversion of this idea into a pixel device is shown in Figure 13. It depicts a 12 tip gated field emitter array in which the gate is connected to a bi-material thermal actuator that is thermally isolated from the substrate and anchored to the silicon substrate. The two anchors are not shown in the Figure. The IR signal enters through the back of the chip (which is transparent to IR) and heats the gate plate, which is covered with a thin IR absorbing layer. The heat travels to the bi-material activator, which causes a deflection of the gate that is proportional to the incident IR radiation.

The readout system consists of a cathode ray tube (CRT) phosphor plate. The phosphor brightness is linearly proportional to the emission current. In an $n \times m$ pixel array, all of the gates are connected. Temperature compensation is achieved by measuring the temperature and then adjusting the gate voltage for a dark image with no IR radiation reaching the DVIR chip.

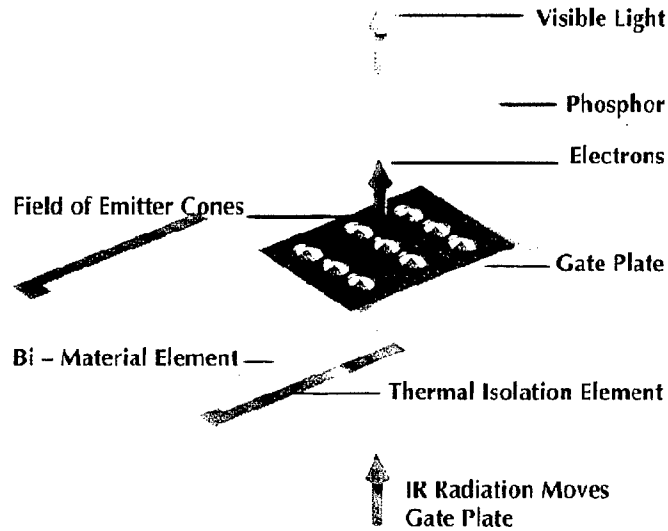


Figure 13. Perspective view of one of the pixel elements. The incident IR radiation is absorbed in the gate plate and increases the temperature of the bimaterial arm which causes the gate plate to deflect. The gate is thermally isolated by a SiC cantilever that is anchored to the substrate. (Anchors not shown.)

3.2 Sensitivity

At present, no experimental results exist showing the emission current as a function of gate movement. There are several publications reporting emission currents at different gate positions -- in which the gates are anchored to the interdielectric layer and tip-to-gate distances are varied by changing processing conditions. Ambiguities in the results exist, since emission currents of field emitters with supposedly identical processing conditions can vary significantly from array to array on the same wafer. Nevertheless, emission currents can change by a factor of 3 to 10 for a positional change of $0.3\ \mu\text{m}$ (experimental) [10, 11]. Theoretical calculations in [12] predict a change in emission current by a factor of 10 for a $0.5\ \mu\text{m}$ gate motion.

Theoretical calculations performed at Sarnoff by Dr. David New are summarized below. Two types of field emitters, volcano-shaped gate and tip-on-post, were considered. Figure 14 shows the radial symmetric tip/gate configurations that were used in the calculations and the respective current trajectories. Figure 15 shows the emission currents as a function of gate-tip positions. The tip-on-post configuration is more sensitive. However, at Sarnoff we are only processing the volcano-shaped version at present. For that configuration the emission current changes by an order of magnitude for a $0.6\ \mu\text{m}$ gate motion.

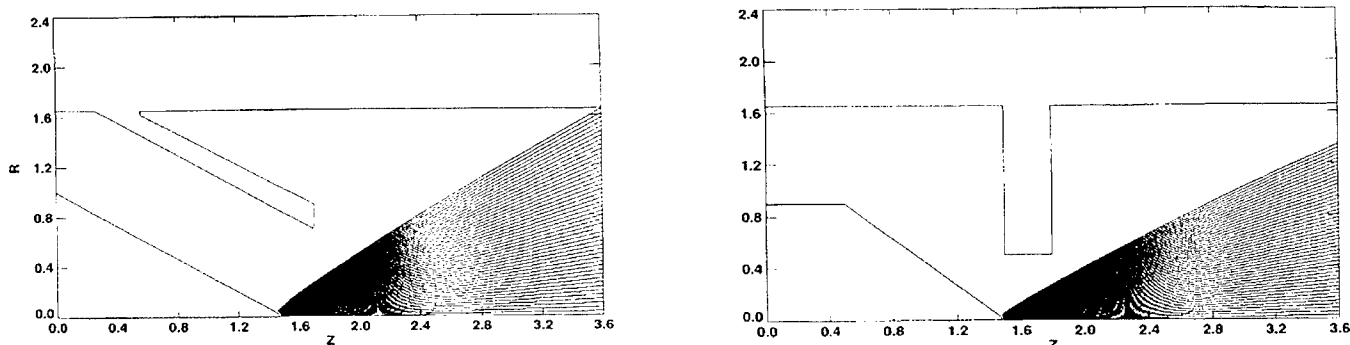


Figure 14. Cross-section and current trajectories of volcano-shaped gate and tip-on-post field emitters that are used in calculating device sensitivity (D. New, Sarnoff).

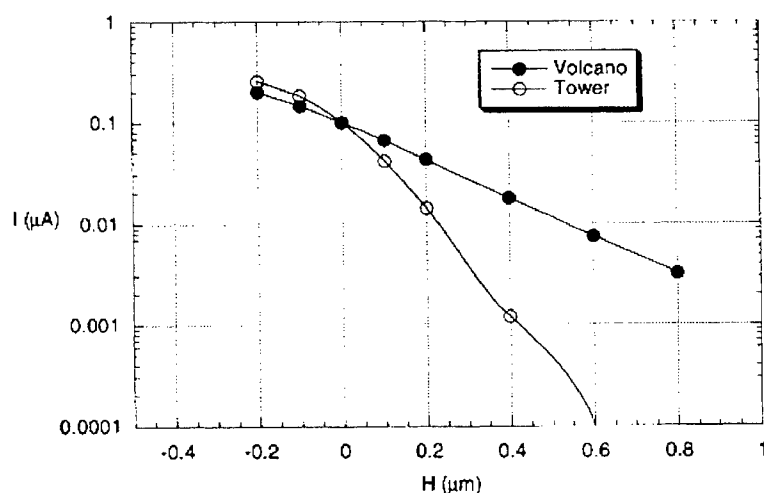


Figure 15. Emission current versus gate-tip position for the two different field emitters in Figure 14.

Recently, Dr. Marek Turowski of CFD Research Corporation, Huntsville, AL under AFRL, SBIR contract F29601-00-0123 has modeled the Sarnoff volcano gate structure for consideration in a MEMS gyroscope [13].

Figure 16 shows the SEM cross-section of the DVIR Sarnoff device, Figure 17 the field distribution for the moving gate at zero position, and Figure 18 the current-position plot. Highest sensitivity is obtained at positive gate positions. Fortunately, that is the case for our experimental devices since, after release, they tend to curve slightly upwards.

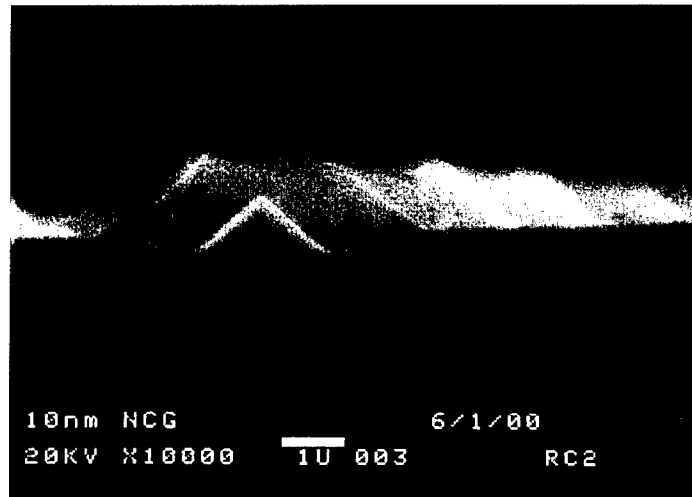


Figure 16. Cross-section of a Sarnoff processed volcano-shaped gated field emitter [13].

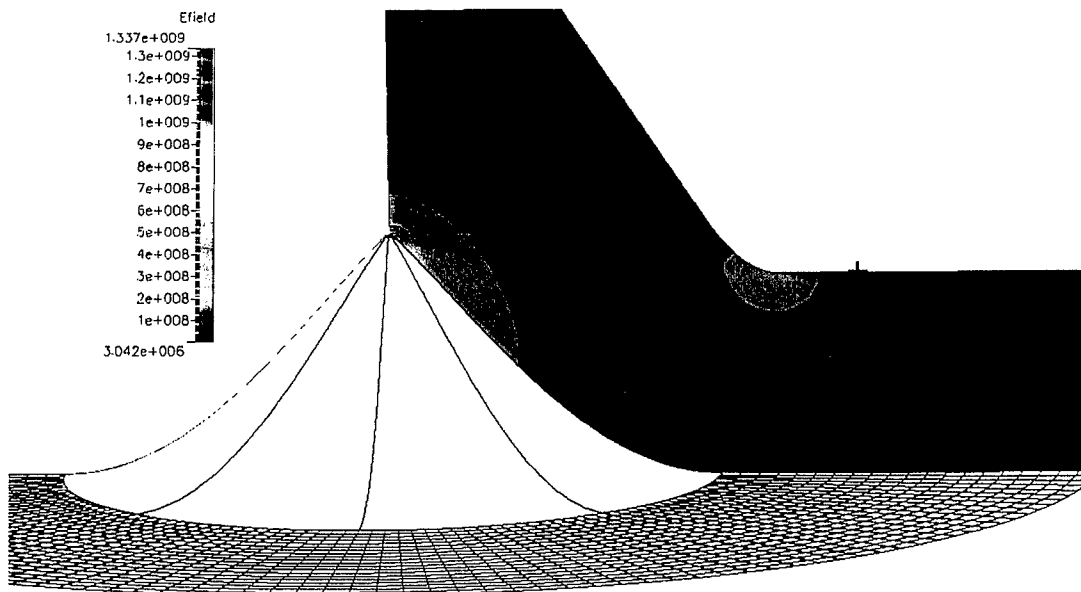


Figure 17. Field distribution of the devices in Figure 16 with the moving gate in zero position [13].

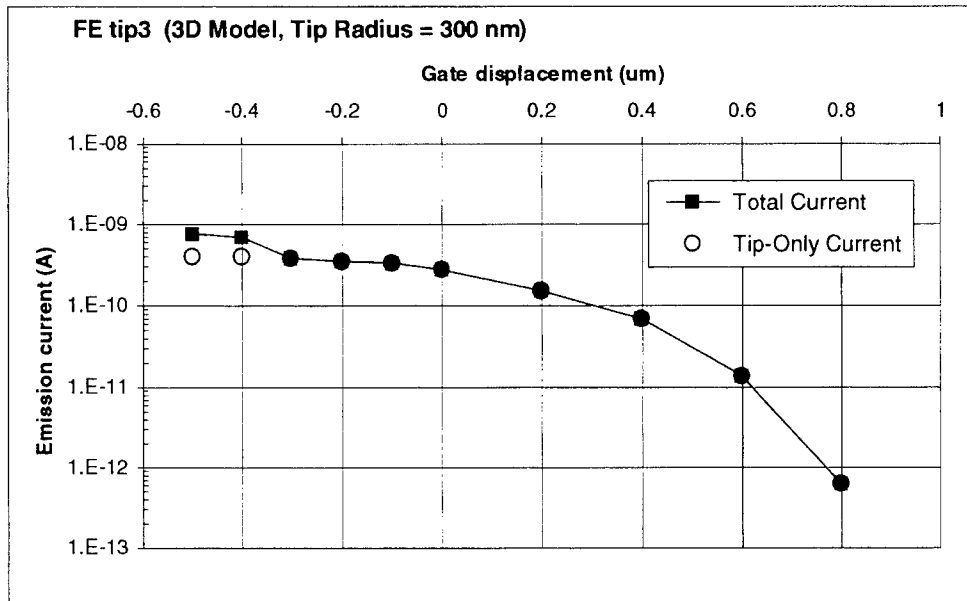


Figure 18. Emission current versus gate position for a device in Figure 16 [13].

What these experimental and theoretical results show is that emission currents should change by about an order of magnitude for gate motions of 0.3-0.6 μm . With expected sensitivities of 0.1-0.2 $\mu\text{m}/^\circ\text{C}$, this corresponds to total temperature changes of 1.5-6 $^\circ\text{K}$.

3.3 Noise Considerations

In our original DVIR proposal, we estimated that with DVIR we could reach a noise equivalent ΔT (NEAT) of about 100 mK. The following assumptions were made:

- The current fluctuations of a single emitter $\Delta I/I \approx 1\%$
- 36 emitters are used in a 50 μm x 50 μm pixel and that $\Delta I/I$ reduces by the square root of the number of emitters
- That $\Delta I/I$ can be reduced by an additional factor of 2 if appropriate thin film surface coatings are used
- The β of the IR system is 100. Here β is the ratio of the temperature at the scene to the temperature at the chip.

As will be shown in the experimental section, some of these assumptions were not correct. Fortunately, an operating window does exist in which $\Delta I/I$ can be reduced significantly, thus coming close to the original estimate of an NEAT of about 100 mK.

3.4 IR Deflection Testing

Once DVIR devices were released and dried using the supercritical CO₂ method, the deflections of the MEMS gates were monitored using a computerized optical profilometer (Phase Shift Technology). Using the same test apparatus, test probes could then be positioned via XYZ manipulators to contact the substrate, gate and shield of individual devices or of arrays. By applying different biases, pull-in experiments (typical to the one shown in Figure 8) could be performed.

To obtain IR deflection measurements, the DVIR chip was mounted on a specially designed sample holder capable of directing an incoming 10.6 μm IR laser beam through the back of the silicon chip. Deflection was then monitored as a function of IR power. The IR power could be varied using an attenuator. The same system was also used to monitor IR deflection inside the vacuum system. Figure 19 shows the schematic of the CO₂ laser system as it was attached to the high vacuum system and Figure 20 a close-up of the sample holder. When the system was used for profilometer measurements, the sample holder, attenuator, and laser were removed from the vacuum chamber and reassembled at the optical profilometer station.

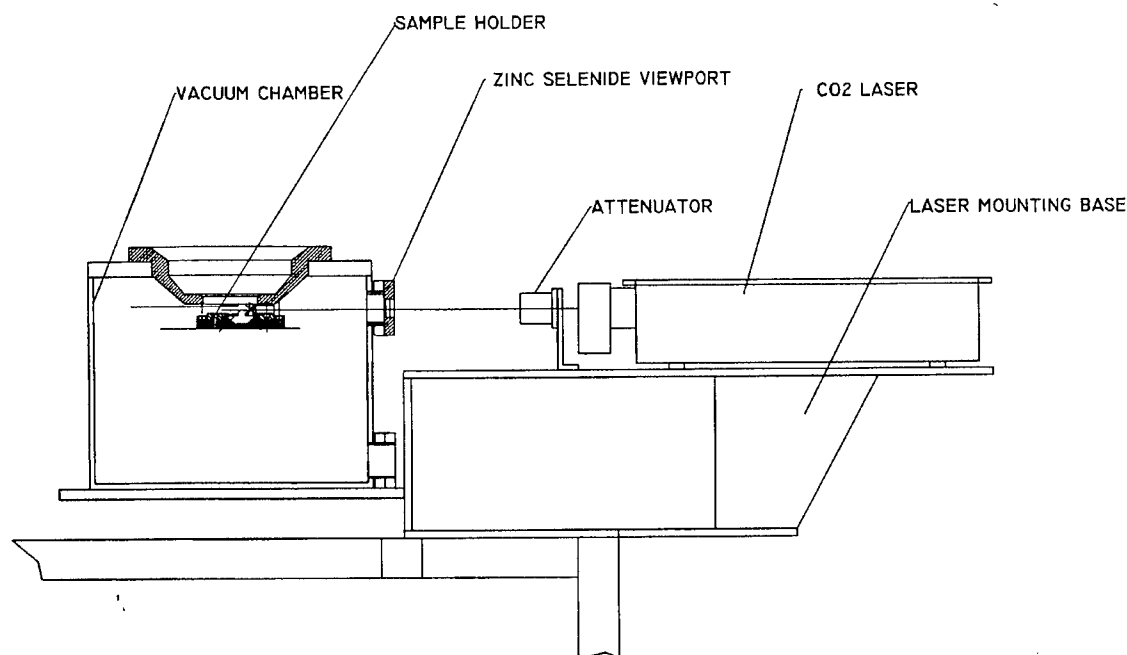


Figure 19. Schematic of the CO₂ laser system for IR deflection measurements.

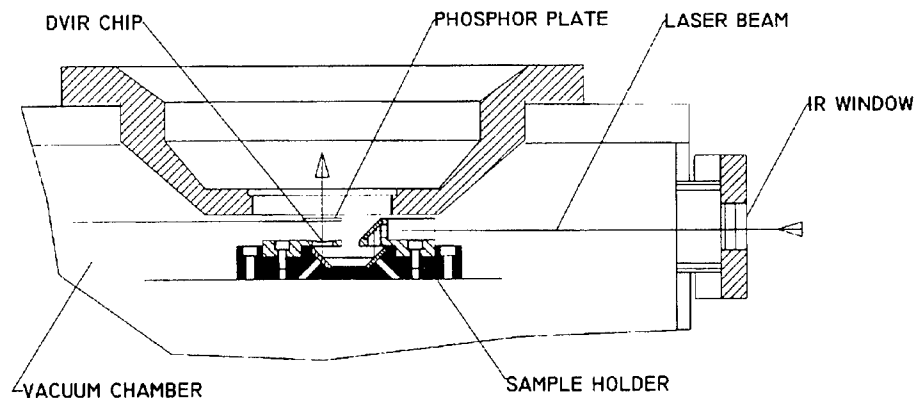


Figure 20. Enlarged view of the sample holder that was used for IR deflection measurements in the vacuum system and in the optical profilometer system.

Figure 21 shows a typical result of an IR deflection measurement as obtained with the optical profilometer. The top three images show the top view of a single-tip cantilever (top left), the perspective view of that cantilever (top right), and the deflection of one of the cantilever arms to which the gate plate is attached. The total deflection of that 70 μm long cantilever arm is only 0.7 μm . As this device is actuated with 10.6 μm IR radiation of 1.2 W incident energy on the back of the chip, the gate moves downwards by about 0.7 μm . This downward motion is clearly discernible from the bottom images. Based on the sensitivity calculation in 3.2, this downward motion should result in a 1 order-of-magnitude change in the field emission current.

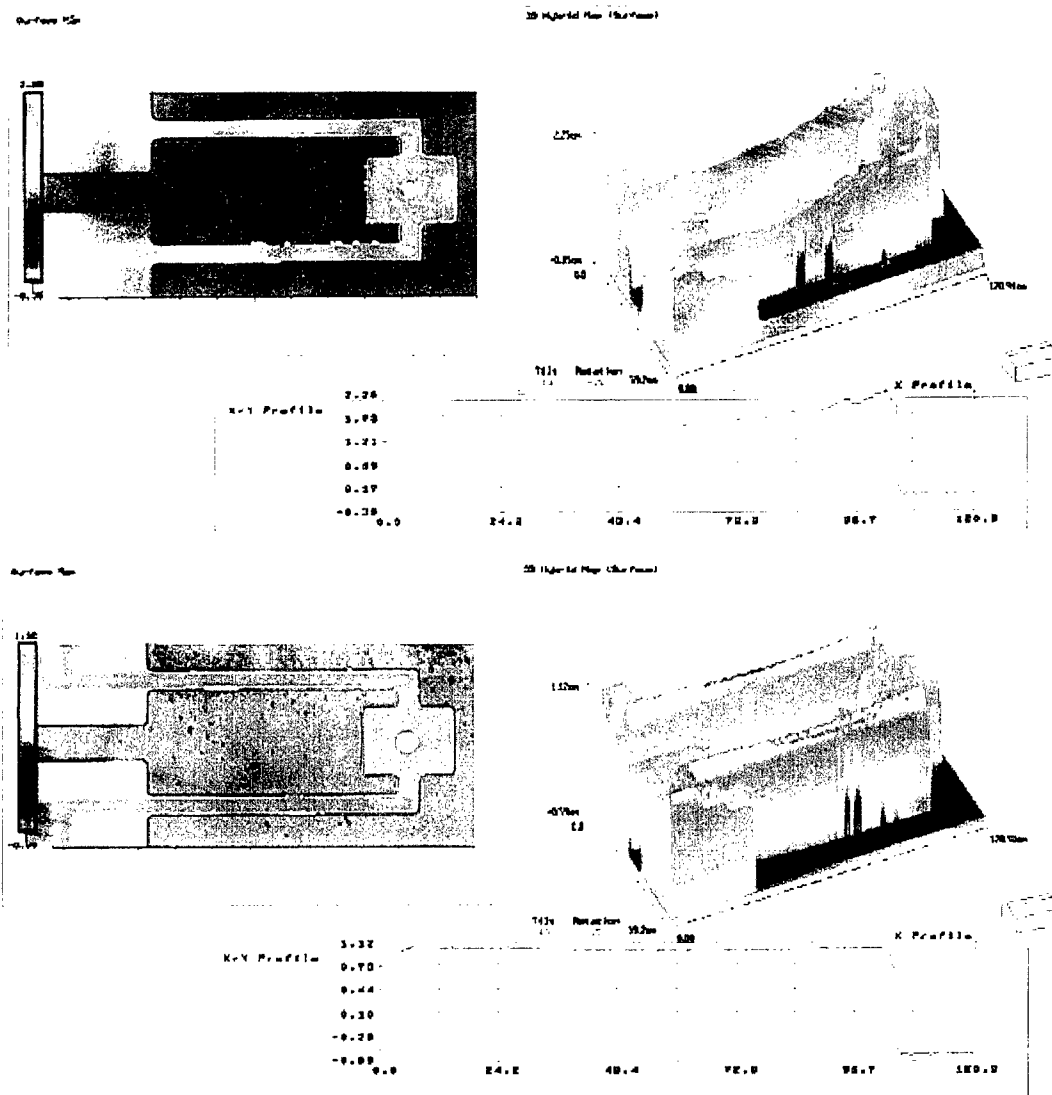


Figure 21. Top view, perspective view and height profile of a 70 μm long cantilever without (top images) and with 10.6 μm IR activation. The gate moves toward the tip by about 0.7 μm when IR activated. The laser input power was 1.2 W. This corresponds to a sensitivity of -1.2 μm/W/100 μm. (Deflection increases by $(100/70)^2$ when normalizing to a 100 μm long cantilevered arm).

3.5 Field Emitter Testing

The DVIR field emitters were tested in a high vacuum test station that was equipped with 3 XYZ manipulators. Two of them contained tungsten probes with 25 μm probe radii. These were used to contact the gates and the shields of the devices. Ground contact was provided through the chip and the stainless steel sample holder that is shown in Figure 20. The third manipulator contained a glass substrate that was coated with indium tin oxide and a green CRT phosphor. After contacting the appropriate device with the two probes, the phosphor plate was moved over the device so that the electron-induced phosphor image could be observed. Placement of the

probes was monitored through a high-power microscope positioned on the outside of the vacuum chamber.

To reduce turn-on voltages of the silicon tips by *in situ* hydrogen reduction of the native oxide, a hydrogen plasma system was designed, fabricated, and installed. The construction of the system was similar to that of Prof. Pryor's of Wayne State University. He uses a similar system prior to boron nitride deposition. Figure 22 shows the schematic of the hydrogen plasma system.

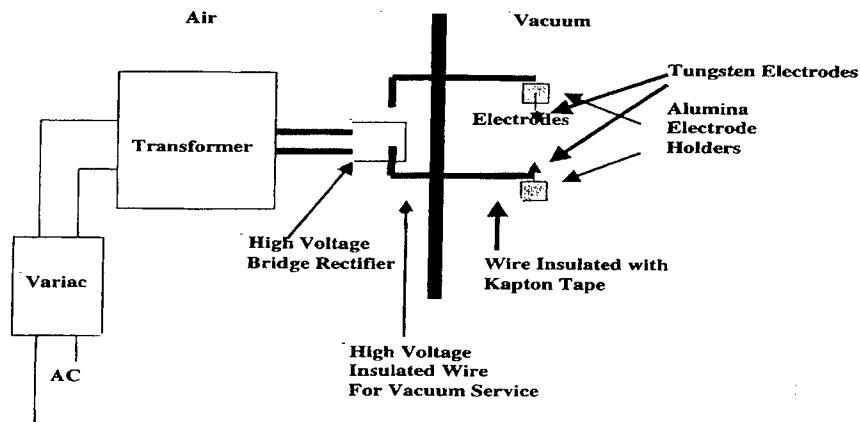


Figure 22. Schematic of the hydrogen plasma system for the reduction of the native oxide on silicon tips.

3.6 Device processing

The first mask set was designed in November 1998. It consists of individual pixel elements with 1, 5, 10, 20, and 30 emitters with cantilever widths of 3, 4, 5, and 6 μm . The cantilever lengths are 40, 60, and 100 μm . Two devices per group of parameters were fabricated. For these devices, the actuator length was half of the cantilever length. In some of the devices, the actuators were fabricated over the entire cantilever length. A small group of devices have gate shields. The device shown on Figure 21 has the actuator extended over the entire cantilever. Deflection of this kind of device is parabolic. This is acceptable if only one emitter or one row of emitters per gate is used. However, when an array is used, only one line of emitters will contribute most of the current. To investigate parallel plate motion, some devices with 100 emitters/plate and 4 actuators moving the plate were included in the mask set. Figure 23 shows the overall layout of the first mask set. In addition to these devices, devices to measure the lateral thermal resistance of SiC were included, as well as sharper tip emitters and diagnostic devices for stress gradient evaluation. Appendix A describes this mask set in detail and outlines our initial processing strategy.

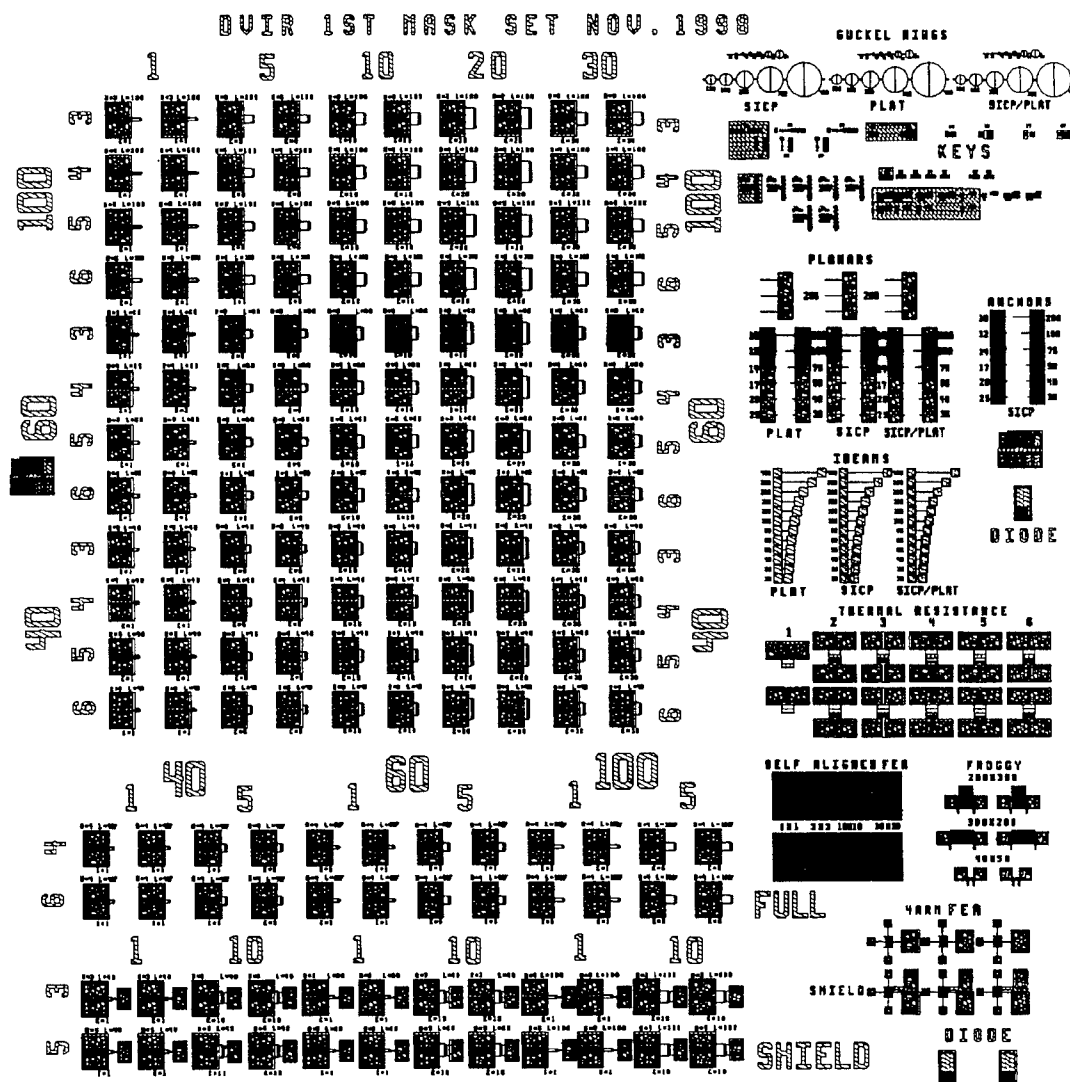


Figure 23. Layout of the test patterns for DVIR proof of concept phase.

The strategy for the second mask set was to obtain at least **one** 16 x 16 array for which proof-of-principle -- namely, modulation of the phosphor image with incoming IR power -- could be demonstrated. The mask set contains eighteen 16 x 16 arrays with different cantilever lengths and numbers of emitters per array. To increase pull-in voltages, in some arrays, the TiW gate connection was decoupled from the bimaterial activator. This minimizes pull-in capacitance. In case gate-to-substrate shorts exist in the 16 x 16 arrays, for each array, a 1 x 4 array and a single pixel array have been included in the mask. This allowed us to evaluate the performance of a given design. A lift-off mask was included to place an absorber on top of the SiC plates for some select devices.

QUIRZ DEVICE LOCATION MAP

The diagram is a floor plan titled "QUIRZ DEVICE LOCATION MAP". It shows a complex layout of rooms and corridors. The rooms are numbered as follows:

- Top row: 1, 2, 3, 4, 5, 6
- Second row: 7, 8, 9, 10, 11
- Third row: 12, 13, 14, 15, 16
- Fourth row: 17, 18, 19, 20
- Bottom row: 21, 22, 23, 24

Other labeled areas include:

- KEYS (near room 17)
- 71, 69, 48, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100
- 61, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83, 84, 85, 86, 87, 88, 89, 90, 91, 92, 93, 94, 95, 96, 97, 98, 99, 100

The diagram also includes a legend in the bottom left corner:

- 1. QUIRZ DEVICE
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- 100. QUIRZ DEVICE

24

Table 2. DVIR 2 Device List.

DVIR2 DEVICE LISTING AND DESCRIPTION

Number	ARM size	Shield dia.	Array size	emitters/array	pads	Name
1	10	4	16x16	15	2	10um_s_16x16
2	15	4	16x16	15	2	15um_s_16x16
3	20	4	16x16	15	2	20um_s_16x16
4	50	4	16x16	15	2	50um_s_16x16
5	38	4	16x16	12	2	wmc3_s_16x16
6	n/a	n/a	3x4	400	1	20x20_fea_array
7	10	2	16x16	15	2	10um_s2_16x16
8	15	2	16x16	15	2	15um_s2_16x16
9	20	2	16x16	15	2	20um_s2_16x16
10	50	2	16x16	15	2	50um_s2_16x16
11	n/a	n/a	2x6	n/a	13	test_fuses
12	10	4	16x16	15	4	10um_tss_16x16
13	15	4	16x16	15	4	15um_tss_16x16
14	20	4	16x16	15	4	20um_tss_16x16
15	n/a	n/a	single	10000	1	1kx1k_paddle
16	50	4	16x16	15	2	50um_da_s_16x16
17	100	4	16x16	15	2	100um_da_s_16x16
18	50	4	16x16	15	4	50um_tss_16x16
19	10	4	1x4	15	2	10um_s_1x4
20	15	4	1x4	15	2	15um_s_1x4
21	20	4	1x4	15	2	20um_s_1x4
22	50	4	1x4	15	2	50um_s_1x4
23	10	2	1x4	15	2	10um_s2_1x4
24	15	2	1x4	15	2	15um_s2_1x4
25	20	2	1x4	15	2	20um_s2_1x4
26	50	2	1x4	15	2	50um_s2_1x4
27	10	4	1x4	15	4	10um_tss_1x4
28	15	4	1x4	15	4	15um_tss_1x4
29	20	4	1x4	15	4	20um_tss_1x4
30	50	4	1x4	15	4	50um_tss_1x4
31	55	4	1x4	30	4	dvirmc_1x4
32	55	2	1x4	30	4	dvirmc_s2_1x4
33	50	4	1x4	15	2	50um_da_s_1x4
34	100	4	1x4	15	2	100um_da_s_1x4
35	38	4	1x4	12	2	wmc3_s_1x4
36	38	4	single	6	2	wmc2_s_single
37	38	4	single	12	2	wmc3_s_single
38	38	4	single	2	2	wmc4_s_single
39	20	4	single	6	3	wmc_s_single
40	10	4	single	15	2	3x5_10mcS_single
41	15	4	single	15	2	3x5_15mcS_single
42	20	4	single	15	2	3x5_20mcS_single

43	50	4	single	15	2	3x5_50mcS_single
44	10	2	single	15	2	3x5_10mcS2_single
45	15	2	single	15	2	3x5_15mcS2_single
46	20	2	single	15	2	3x5_20mcS2_single
47	50	2	single	15	2	3x5_50mcS2_single
48	55	2	16x16	30	3	dvir_s2_16x16
49	55	2	single	30	3	dvir_s2_single
50	55	4	single	30	3	dvir_s_single
51	50	4	single	15	2	3x5_50dmc_s_single
52	100	4	single	15	2	3x5_100dmc_s_single
53	30	4	single	15	2	1x1_30dmc2
54	38	4	single	1	3	wmc4_ms_single
55	10	4	single	15	4	3x5_10mc_tss_single
56	15	4	single	15	4	3x5_15mc_tss_single
57	20	4	single	15	4	3x5_20mc_tss_single
58	50	4	single	15	4	3x5_50mc_tss_single
59	n/a	n/a	single	1200	1	fea2
60	n/a	n/a	single	1	1	fea3
61	55	2	16x16	30	3	dvirmc_a_16x16
62	38	4	16x16	12	2	wmc3_s_a_16x16
63	n/a	n/a	2x2	3000	8	2x2_fea
64	38	4	1x4	12	2	wmc3_s_a_1x4
65	38	4	single	12	2	wmc3_s_a_single
66	55	4	single	30	3	dvir_single_a
67	55	4	1x4	30	4	dvirmc_a_1x4
68	105	4	single	48	3	dvir_ti_single
69	105	2	single	48	3	dvir_ti_s2_single
70	n/a	n/a	test	n/a	?	test1
71	n/a	n/a	test	n/a	?	test2
72	n/a	n/a	single	6000	?	60x80fea_s2
73	n/a	n/a	single	6000	?	60x80fea_ng

Figure 25 shows the top view of one pixel element in which the gate shield only surrounds the 30 emitter area and not the absorber. The actuator is electrically decoupled from the 20 nm thick TiW gate metallization. The device can also be modulated via the pull-in contact. The pull-in connection is also electrically decoupled from the gate contact. A TiW cross bar is shown in the absorber plate. It connects the two gold-TiW/SiC actuators so that symmetrical pull-in of the structure is obtained when the pull-in contact is actuated. The strategy of adding the pull-in contact was selected in case the device could not be modulated by IR due to insufficient IR absorption in the SiC layer. Field emitter modulation via a moving gate could still be demonstrated.

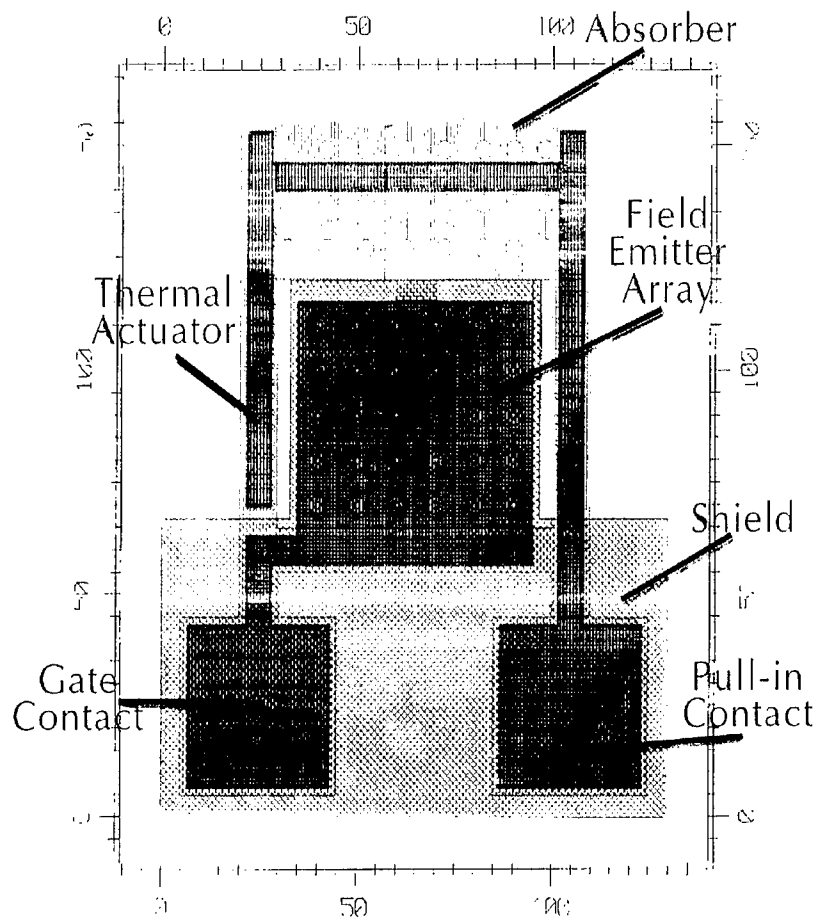


Figure 25. Top view of a single pixel device in which the emitter array is electronically isolated from the bimaterial gate activator. In addition to the IR activation, the gate can be moved with respect to the emitter tips by applying a bias to the pull-in contact with respect to the substrate. The SEM micrograph of this device is shown in Figure 2 (top) and a section of this device within an array is shown in Figure 2 (bottom).

The process will be described with reference to Figures 2 and 25. The cross-section of such a device is shown in Figure 26.

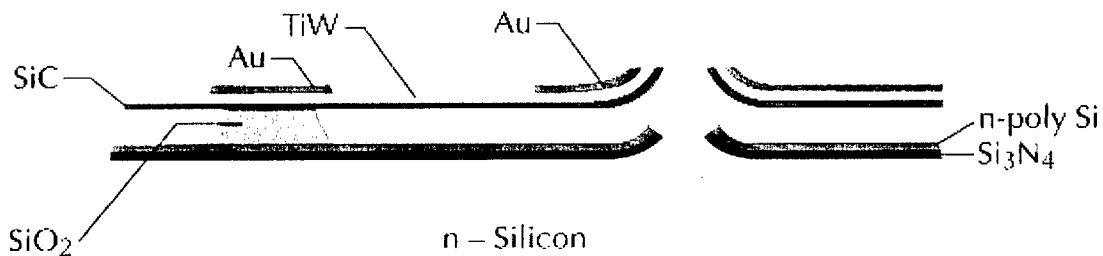


Figure 26. Cross-section of a shielded device.

Processing starts with a lot of 25, 4-in., n-type Si wafers. Thin layers of SiO_2 and Si_3N_4 are grown/deposited and the necessary alignment keys are fabricated. This is followed by photoresist application and the definition of 6 μm diameter islands. The silicon is then etched isotropically in CF_4/O_2 until small plateaus (0.2-0.5 μm) remain on top of the tips. The photoresist is removed, the wafers are cleaned and a 0.85 μm thick steam oxide is grown. During this process, the tips are being sharpened. The oxide is then removed in buffered HF and 1000 Å of SiO_2 , 1500 Å of Si_3N_4 and 2000 Å of LPCVD polycrystalline silicon are grown/deposited. Depending on if a reflective IR shield or a transparent IR shield is chosen, the polycrystalline silicon is either POCl_3 doped, or phosphorus ion implanted and activated. A photomasking step is performed next to define the gate shield holes around the tips. The polycrystalline silicon layers and the Si_3N_4 are dry etched. Etching stops at the 1000 Å SiO_2 layer. This layer is necessary to avoid etching of the tips. After photoresist stripping and cleaning, a 0.85 μm thick layer of PCVD oxide is deposited. This layer serves as the anchor material and the sacrificial layer. On top of the oxide, 2500 Å thick SiC, 200 Å TiW, and 3000 Å Au are deposited and photo defined by first etching the gold, followed by TiW definition and etching, followed by SiC definition and etching. After photoresist stripping, the devices are ready for release etching and supercritical CO_2 drying.

Release etching is performed in concentrated buffered HF that does not contain an additional wetting agent. It was found that the wetting agent removed the TiW after 40 minutes into the process. Prior to release etching, appropriately sized chips are broken off the wafer by using a diamond scribe. These chips are then inserted into a beaker and bHF etched for about 75 minutes. This is the necessary time to release the structure in Figure 2. The chip is then carefully lifted out of the beaker into a dish containing DI wafer and stays there for about a minute. After that it is transferred into a methanol containing dish and inserted into the CO_2 drying apparatus, in which the drying chamber contains methanol. The CO_2 apparatus was purchased from GT Equipment Technologies, Inc., Nashua, NH. In the chamber, methanol is replaced by liquid CO_2 which is then transferred into its supercritical state by elevating the pressure and temperature in the chamber. After the process is finished, the chips are ready for testing.

4. Results and Discussion

The results are listed in chronological order and include issues related to device fabrication, pull-in, IR activation, and field emission.

4.1 Initial Devices, First Mask Set

4.1.1 SiC/Cr Actuators

The initial devices were fabricated using 3500 Å SiC/100 Å TiW/4000 Å Cr. Figure 27 shows a released, single emitter device of this type in which the actuator covers about half of the cantilever. The thermally isolating arm consists of 3500 Å SiC and 100 Å TiW. The thin layer of TiW is needed to provide an electrical contact to the gate. Figure 28 shows a close-up of the tip/gate region and Figure 29 the first field emission results.

Initial field emitter testing was performed on partially released structures, since in fully released structures the gates were several microns removed from the tips. Emission was obtained for single-tip, and 5, 10, and 100 tip devices. In Figure 29, I-V characteristics of a single-tip at room temperature (RT) and that of a 100 tip device at RT and 340 °C are shown.

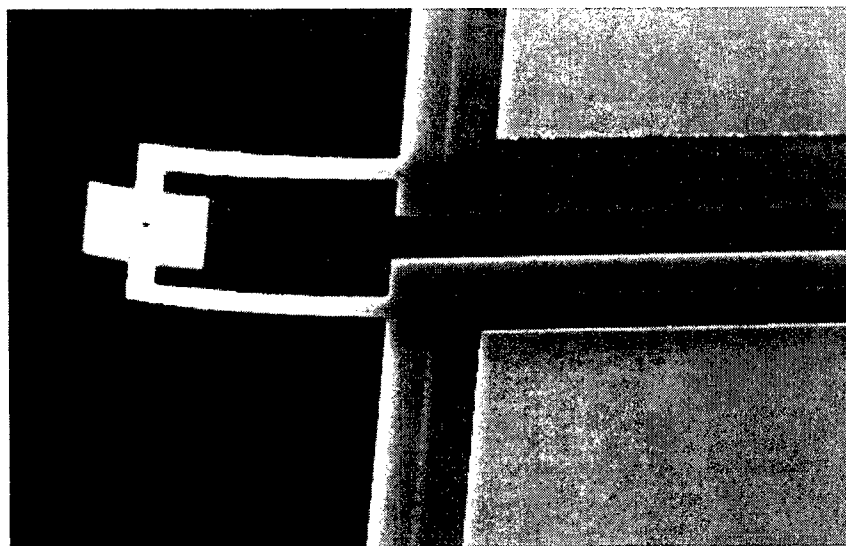


Figure 27. SEM micrograph of a fully-released bimaterial gate (4000Å Cr/ 100Å TiW/ 3500Å SiC), single-tip device. The two darker halves of the cantilevers consist of 3500Å SiC and 100Å TiW. The cantilever length is 40 μm, the width is 6 μm.



Figure 28. SEM micrograph of a single-tip gated field emitter with a $0.4\text{ }\mu\text{m}$ thick Cr gate (inner rim). The gate diameter is $1.4\text{ }\mu\text{m}$.

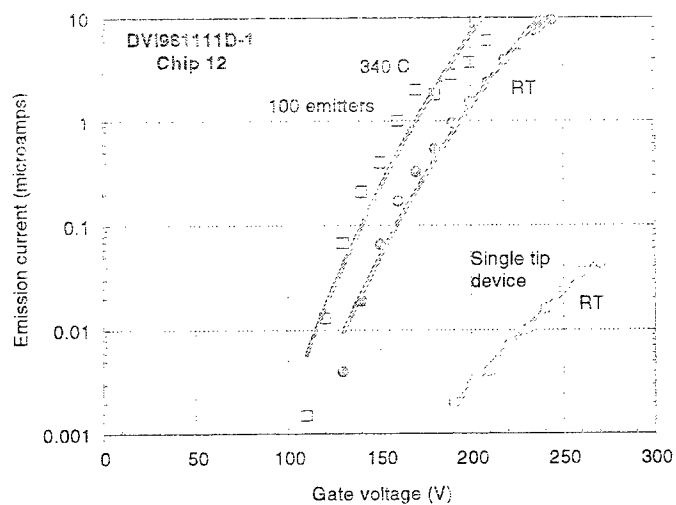


Figure 29. I-V characteristics of a single-tip device at RT and of a 100-tip device at RT and $340\text{ }^{\circ}\text{C}$ taken from DVI981111 D-1, chip 12. The chip was etched in buffered HF for 10 min. to remove the oxide from the tips and CO_2 dried.

Figure 30 shows the phosphor image of a single-tip device and the SEM micrograph of the device from which the image was taken.



Figure 28. SEM micrograph of a single-tip gated field emitter with a 0.4 μm thick Cr gate (inner rim). The gate diameter is 1.4 μm .

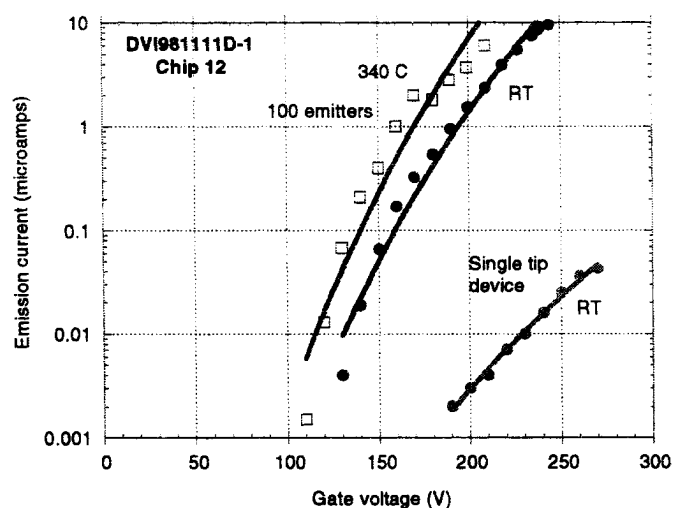


Figure 29. I-V characteristics of a single-tip device at RT and of a 100-tip device at RT and 340 $^{\circ}\text{C}$ taken from DVI981111 D-1, chip 12. The chip was etched in buffered HF for 10 min. to remove the oxide from the tips and CO_2 dried.

Figure 30 shows the phosphor image of a single-tip device and the SEM micrograph of the device from which the image was taken.

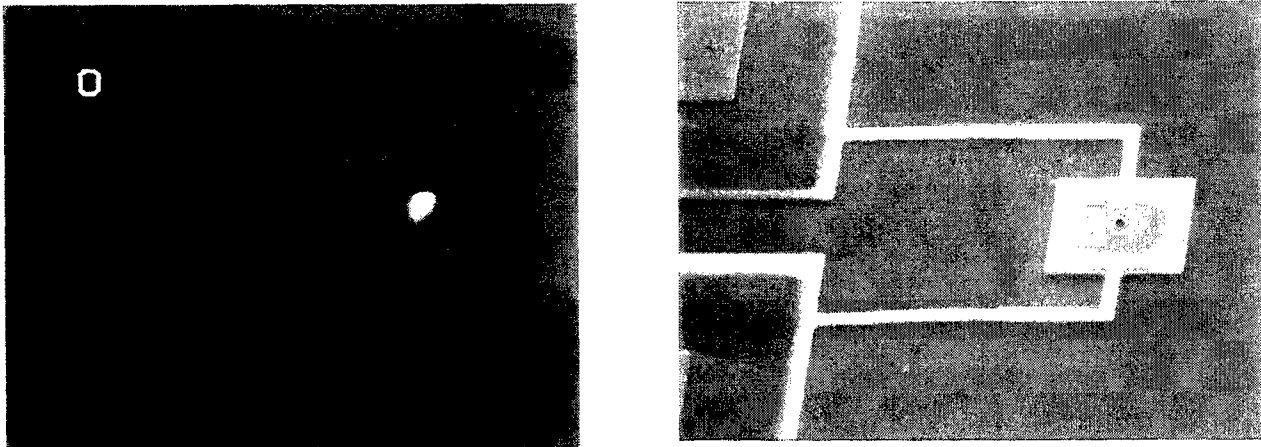


Figure 30. Phosphor image of a single-tip device at a phosphor voltage of 5000V and an emission current of 60 nA (left image) and SEM micrograph of the device from which the emission measurements were taken.

4.1.2 Trenched Devices

Initial pull-in tests of devices in Figures 27 and 30 revealed pull-in voltages ranging from 30-40 V. To increase the pull-in voltages, some devices with trenches were fabricated. Trenches decrease the cantilever-to-substrate capacitance. Figures 31 and 32 show two examples of trenched devices with SiC/Cr actuators.

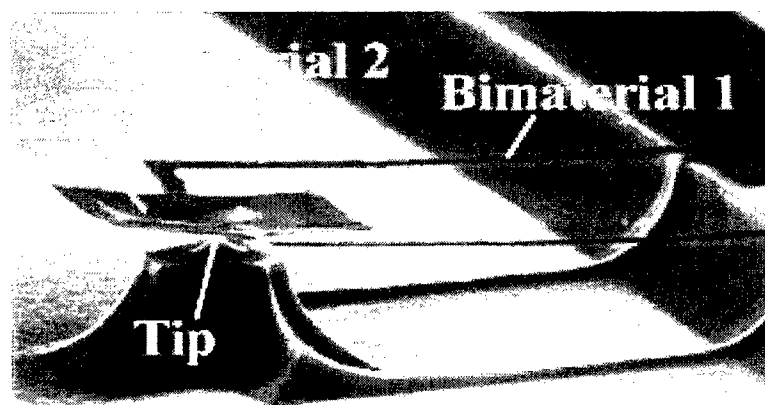


Figure 31. SEM micrograph of a trenched device fabricated by using a 1 μm thick PCVD oxide layer on top of the cantilever as the protective layer during trench etching. The TiW layer disappeared and the Cr was attacked during the process.

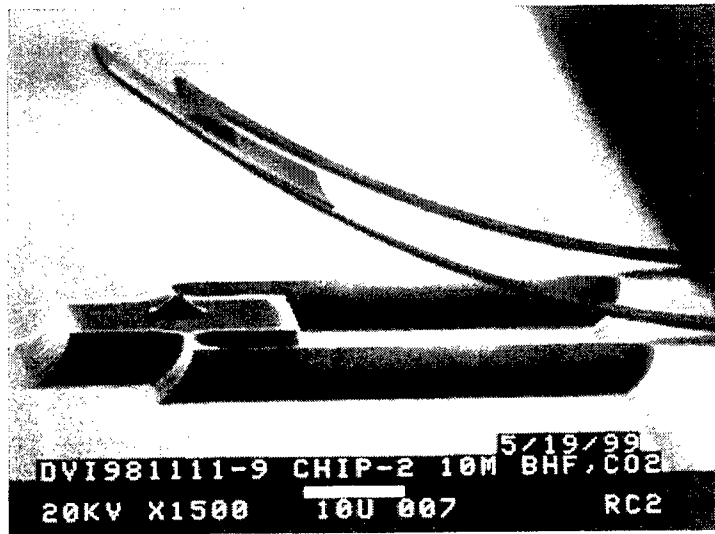


Figure 32. SEM micrograph of a trenched device fabricated by using photoresist as the protective layer during trench etching. The Cr layer disappeared, the TiW layer was not damaged.

Pull-in tests could only be performed from structures in Figure 32, since the actuators in Figure 31 were not electrically conductive due to the missing TiW. Figure 33 shows the pull-in results for devices with three different cantilever lengths.

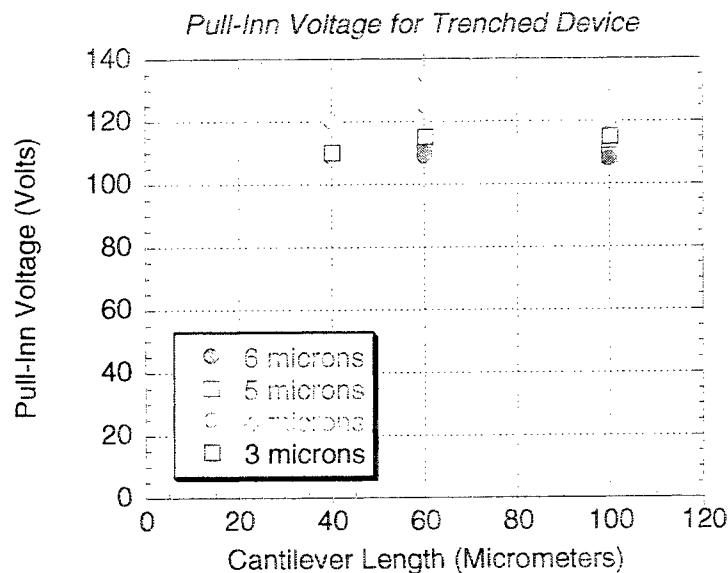


Figure 33. Pull-in voltages versus cantilever length for 3, 4, 5, and 6 μm wide cantilevers of devices similar to the one shown in Figure 32.

The results in Figure 33 are contrary to theory, which predicts the decrease of pull-in voltages with increasing length. Evidenced here is that pull-in is dictated by the small distance of the cantilever near the anchor region with respect to the silicon substrate. This region has identical cantilever curvature independent of the length of the cantilever. From these experiments and the

fact that, for a DVIR product, trenches would be hard to implement, further development of trenched devices was abandoned.

From these initial experiments, the following information was gained:

- Film stresses were too high.
- Sensitivity of gate motion was too low at $0.01 \mu\text{m}/^\circ\text{C}/50 \mu\text{m}$ cantilever.
- Gate moved in the wrong direction.
- Turn on voltages were too high, especially for single-tip devices.
- Temperature dependence of field emission is acceptable since for a DVIR product, the maximum temperature change will only be a few degrees.
- Trenched devices offer small advantages for leveraged cantilevers.

Conclusion – Abandon Cr, find ways to lower emission turn-on.

Solution – Switch over to Au actuators, find ways to lower emitter turn-on (BN coating, sharper tips), concentrate on developing gate shields.

4.1.3 SiC/Au Actuators

The Cr definition was done by a lift-off process. Initial Au devices were processed using lift-off of e-beam evaporated Au. These devices had poor adhesion and it was decided to use sputtered gold. To accommodate this change, two of the masks in the initial mask set of nine masks had to be redesigned.

With the sputtered gold, we obtained a thermal sensitivity of $-0.036 \mu\text{m}/^\circ\text{C}/50 \mu\text{m}$ arm. This is by a factor of 3.6 increase over the Cr devices. Upon testing, the cantilever moved in the right direction, i.e., toward the tips. By replacing Cr with Au and optimizing the SiC deposition parameters, near leveraged cantilevers were obtained. The device shown in Figure 21 is an example of a SiC/Au cantilever device.

4.1.4 Devices with Gate Shields

The cross-section of a shielded device is shown in Figure 26. Figures 34 and 35 show top views of a 10 emitter and a 100 emitter device. The shield is shared with 24 devices with cantilever widths of 3 and 5 μm (see Figure 23, lower left, SHIELD). Since the SiC/Au devices are near leveraged, pull-in voltages, which for the SiC/Cr devices ranged from 30-40 V due to their large curvature, were reduced to about 2 V for the SiC/Au actuators. An increase to 10 V was obtained for the shielded devices. The initial shield opening was chosen at 6 μm . Due to the overetching problem referred to in Section 1.3.3, the actual diameter was about 10 μm .

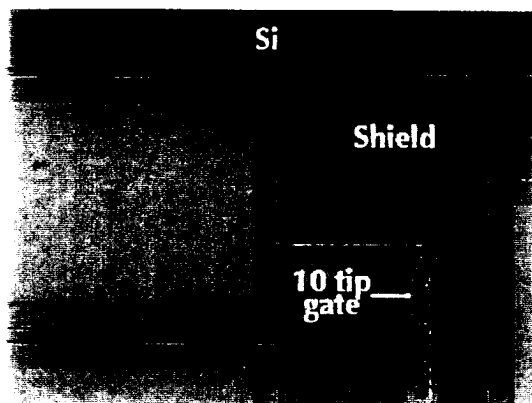


Figure 34. Top view of a shielded 10 tip device.

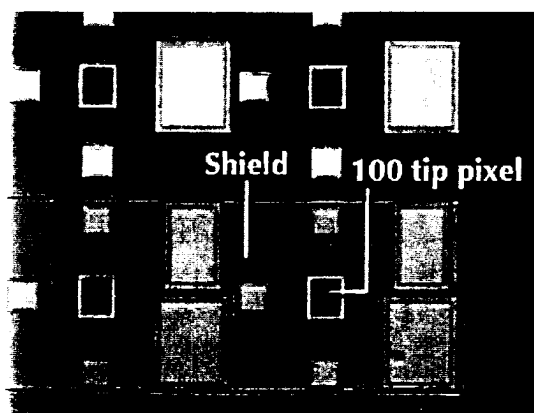


Figure 35. Top view of a shielded 100 tip device. A group of unshielded devices is also fabricated on the same chip. This allows measurements of pull-in voltages for devices with very similar stress gradients and intrinsic stresses.

4.1.5 First IR Activation Experiments (no gate shield)

Figure 36 shows the beam deflection of a 100 μm long 3000 \AA SiC/3000 \AA Au bimaterial arm, in which the gold covers the entire length of the cantilever, as a function of laser power. The laser input power was measured at the exit of the attenuator. At an input power of 520 mW, a deflection of 0.55 μm is obtained. This corresponds to a sensitivity of $-1.1 \mu\text{m}/\text{W}/100 \mu\text{m}$.

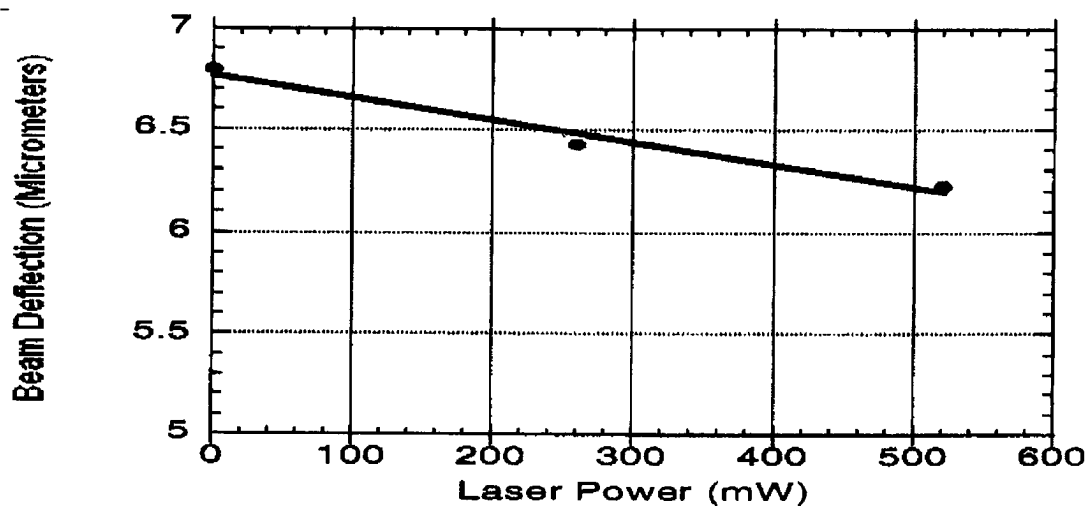


Figure 36. Deflection of a 100 μm long SiC/Au (3000 \AA thick layers) cantilevered DVIR gate as a function of laser power.

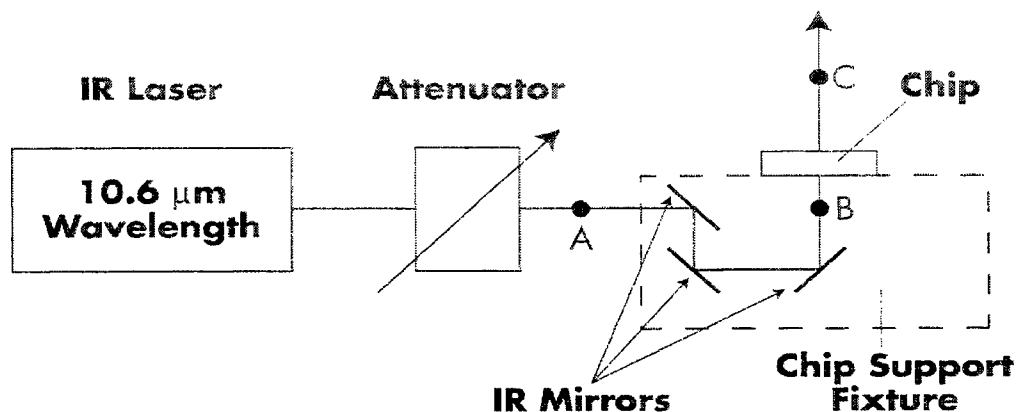
Based on the results from these experiments, the second mask set was designed containing the 16 x 16 pixel arrays. The major changes over the first mask set were stiffer arms and reduced shield holes from 6 μm to 2 μm and 4 μm . In Appendix B, top views of representative patterns are shown. The first is the layout of a 16 x 16 array with an individual pixel element shown in Figure 2. The second is a single plate device in which the gate moves parallel to the substrate and not in a parabolic fashion.

4.2 16 x 16 Arrays, Second Mask Set

The layout of the second mask set and a list of devices have been presented in Section 3.6 and devices from this mask set are shown in Figure 2. Experimental results quoted below and encapsulation work was done with devices from the second mask set.

4.2.1 IR Activation Experiments

Several of the devices were tested using the optical interferometer. Deflection was monitored as a function of IR power at a wavelength of 10.6 μm . Figure 37 shows the test set up. The power from the IR laser can be varied by the attenuator. The particular mirror arrangement is needed to overcome constraints imposed by the test apparatus. The table shows the IR powers measured at different positions. About 15% of the power is transmitted through the chip. If a non-patterned chip is used, about 35% goes through the chip. The difference of 20% is caused by absorption and reflection of the patterns that are fabricated on the chip.



Typical IR Power Measurement

Position	IR Power (W)
A	0.5
B	0.41
C	0.06 (chip with ion implanted shield)

Figure 37. Experimental configuration of the IR activation experiments. The optical interferometer monitors the deflection of the gate plates on top of the chip.

This setup was also used to measure the IR properties of the shields. The power at position B in Figure 37 was set at 200 mW. For a bare n⁺ Si chip, 70 mW is transmitted. For a chip with a POCl₃ shield 10 mW is transmitted. For an ion implanted shield, 65 mW is transmitted. Additional experiments revealed that for a POCl₃ doped polycrystalline Si shield 85% of the IR is reflected and 15% is absorbed.

IR Activation of Single Emitter Device -- Figure 38 shows the SEM of a single-tip device. Deflection was monitored at the outermost edge of the absorber at a distance of 60 μm . With an ion implanted shield, we obtained $-0.27 \mu\text{m}/\text{W}/60 \mu\text{m}$ length and with a POCl₃ doped shield $-0.12 \mu\text{m}/\text{W}/60 \mu\text{m}$. The IR power in Watts is the power at position A in Figure 37.

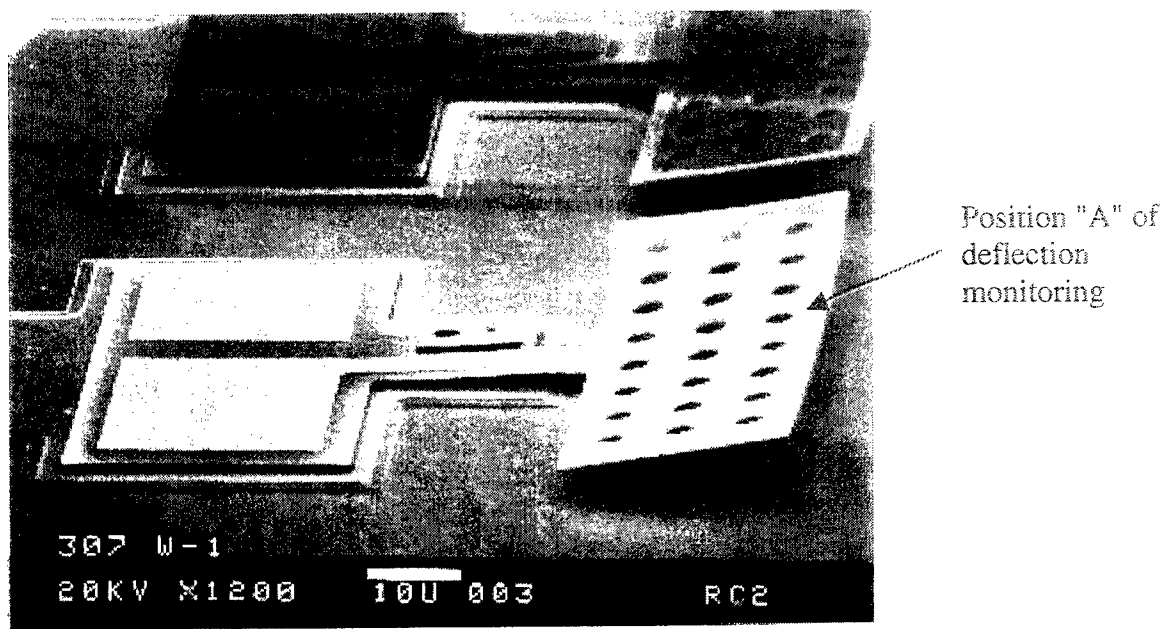


Figure 38. SEM of a single-tip emitter device. Deflection is monitored at a cantilever length of 60 μm (Position A).

The deflection consists of two components. One is heating of the chip and the other one is heating of the SiC absorber. Since the POCl₃ doped shield reflects most of the IR power, the chip is heated less and thus results in a lower deflection sensitivity, i.e., $-0.12 \mu\text{m}/\text{W}/60 \mu\text{m}$ versus $-0.27 \mu\text{m}/\text{W}/60 \mu\text{m}$ for the ion implanted shield. The minus sign indicates downward motion of the gate plate.

Figure 39 shows the deflection versus IR power for the single-tip emitter device in Figure 38. The lower line (with the larger slope of $-0.27 \mu\text{m}/\text{W}/60 \mu\text{m}$) corresponds to measurements when the laser beam was centered at the device. The chip was then moved several mm away from the beam and the measurements were repeated. This is represented by the upper curve (lower slope of $-0.16 \mu\text{m}/\text{W}/60 \mu\text{m}$). Since the device is not exposed to IR power, the deflection has to be caused by heating of the chip.

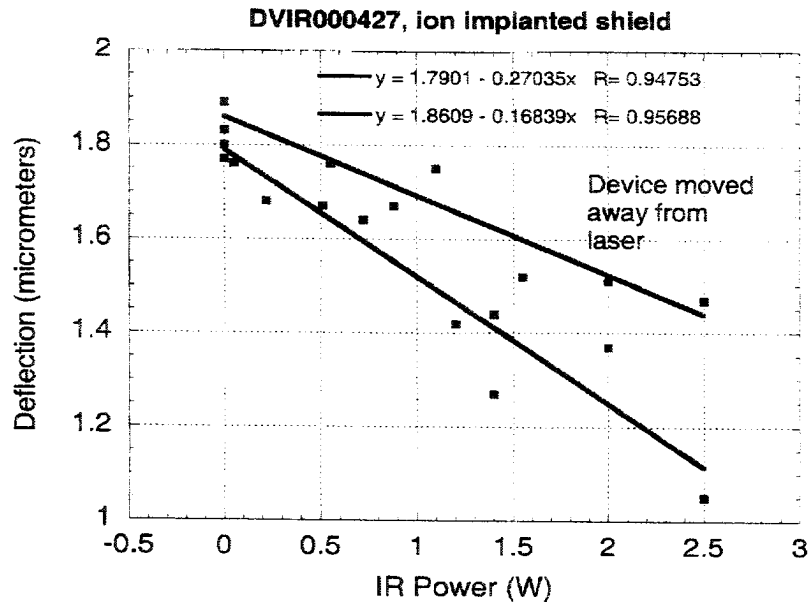


Figure 39. Deflection versus IR power for a single emitter device in which the laser beam is centered with the device (larger slope) and off-centered.

IR Activation of 30 Emitter Devices – Figure 40 shows the deflection of the device in Figure 2 measured at a distance of 110 μm away from the anchor. The sensitivity of this 75 μm long actuator is $-0.19 \mu\text{m}/\text{W}/75 \mu\text{m}$, which normalized to 100 μm is $-0.19(100/75)^2 = -0.34 \mu\text{m}/\text{W}/100 \mu\text{m}$. This is smaller than the $-1.1 \mu\text{m}/\text{W}/100 \mu\text{m}$ obtained for the device from the first mask set. It is believed that the difference is caused by reduced heating of the cantilever due to the reflection of IR power from the POCl_3 doped shield. The device in the first mask set did not have a shield.

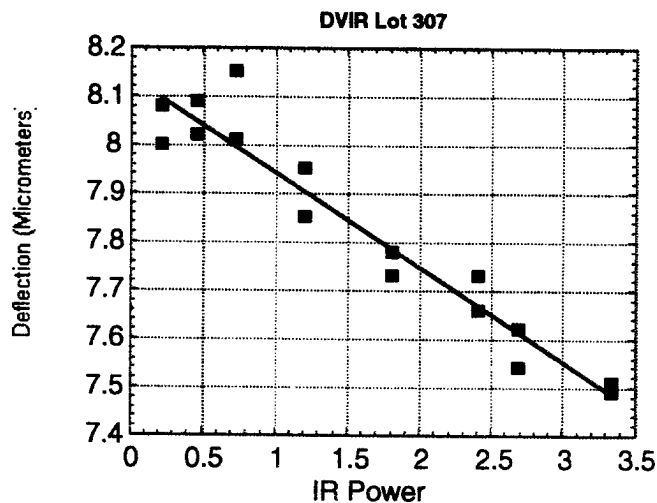


Figure 40. Deflection versus IR power for a 30 emitter pixel element with a POCl_3 doped shield.

4.3 Absorber Experiments

For IR absorption, we relied on the absorbing properties of SiC. There is a lot of room for improvement. Some experiments were performed with black chrome and with poly ethylene glycol-like films.

Prompted by its use as non-reflective surface at low frequency IR region (near the $1\text{ }\mu\text{m}$ region), sputtered black chrome was investigated as an absorber in the $8\text{ }\mu\text{m}$ - $12\text{ }\mu\text{m}$ region. The measurements inferred the absorption properties from the reflection and transmission measurements of the films. We also addressed process integration issues of this deposition step to the existing micromaching process by using a lift-off process.

Film Preparation – The standard low temperature sputtering process from Telic Inc. was used to deposit a $1000\text{ }\text{\AA}$ film of black chrome on three substrates: a potassium bromide piece, a bare silicon piece, and a silicon piece with lift-off resist patterns from a DVIR absorber mask. Potassium bromide is transparent in the IR region of interest and was used for reflection and transmission measurements. The silicon with the resist pattern was used to test compatibility of the deposition with the lift-off process.

Results – The last step of the lift-off process was completed on the resist patterned silicon piece (an acetone rinse step). The mask pattern was transferred to the black chrome with no noticeable defects, indicating good film adhesion and lack of high temperature heating of resist during sputtering.

The black chrome shows strong reflectivity at the wavelength region of interest. The reflectivity is below 10% up to a wavelength of $3\text{ }\mu\text{m}$, but then monotonically increases, reaching 75% at about $8\text{ }\mu\text{m}$. This experiment concludes that the black chrome is not a good absorber for the $8\text{ }\mu\text{m}$ - $12\text{ }\mu\text{m}$ wavelength region. Figure 41 shows the SEM micrograph of a $1000\text{ }\text{\AA}$ black chrome film on silicon processed by a lift-off technique and Figure 42 shows the reflectivity of the $1000\text{ }\text{\AA}$ black chrome film as a function of wave number k .

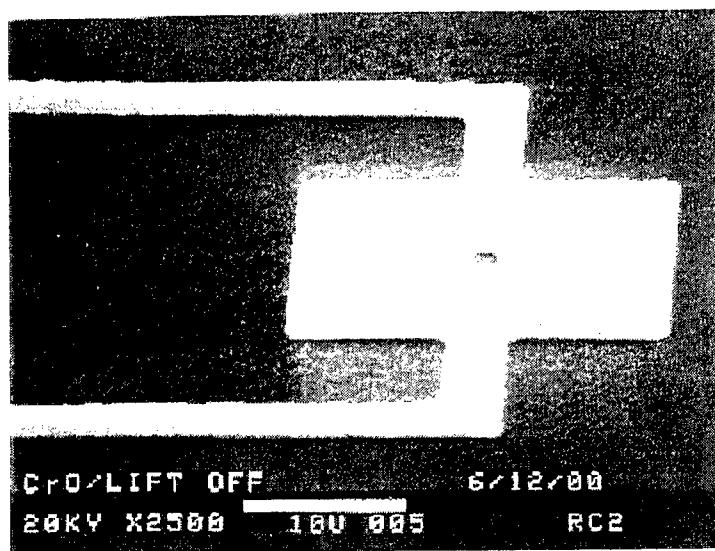


Figure 41. SEM micrograph of a $1000\text{ }\text{\AA}$ black chrome absorber processed by lift-off.

Sarnoff Corp

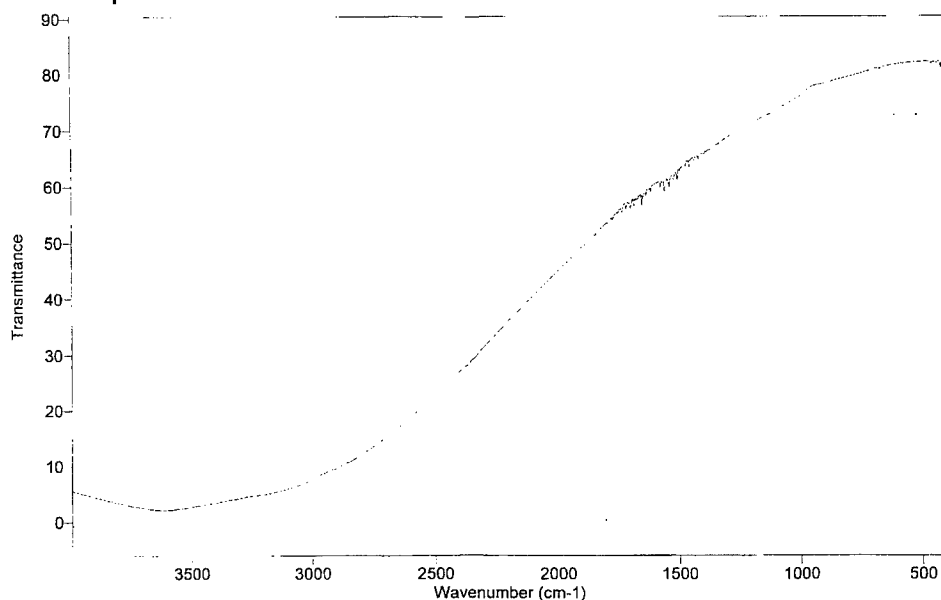


Figure 42. Transmittance spectrum of a 1000 Å thick sputtered black chrome absorber.

Poly Ethylene Glycol – In addition to black chrome, Dr. Jia Ming Chen of our group was working with Dr. Y. Vickie Pan at University of Washington, Seattle on poly ethylene glycol films. Preliminary experiments indicate an absorption peak at 9 μm . At higher wavelengths, absorption decreased. Figure 43 shows the transmittance spectrum of a 1000 Å film.

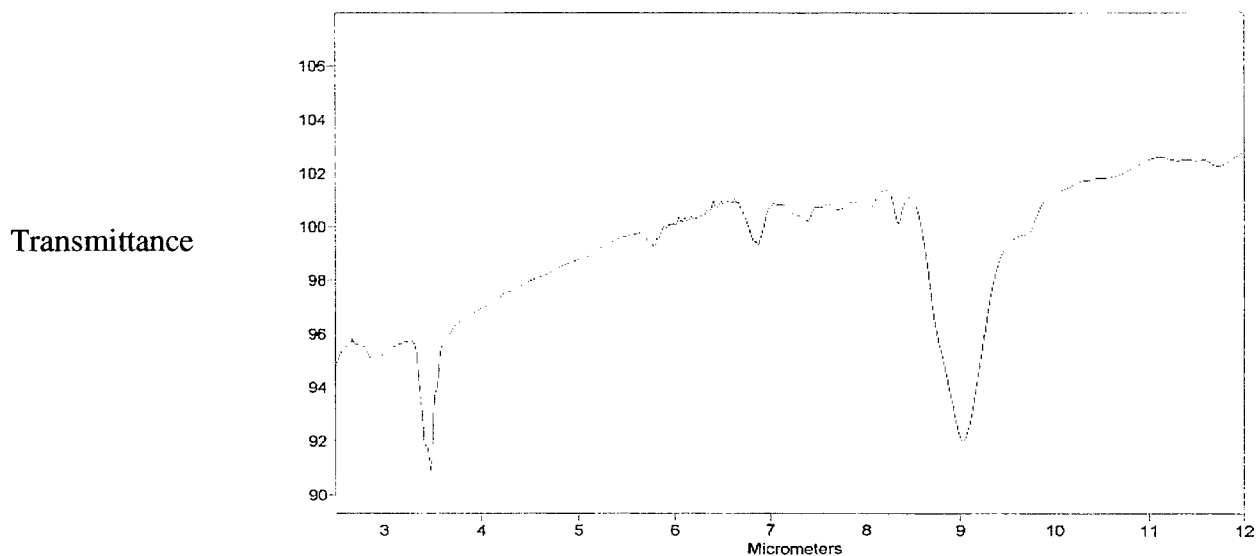


Figure 43. Transmittance spectrum of a 1000 Å thick poly ethylene glycol-like film.

Similar to Figure 41, lift-off experiments were performed and absorbers could be defined.

We also established that 1000 Å thick sputtered BN films have strong absorbing properties but detailed experiments were not performed.

4.4 Low Emitter Turn-on Voltages

As mentioned in the Overview and shown in Figure 5, thin films of BN and nanocrystalline graphite (NCG) can lower turn-on voltages of silicon field emitters drastically. The results in Figure 5 were performed with our standard 6460 tip field emitter array and not with a DVIR chip. Use of NCG for DVIR is not recommended. Since the deposition temperature is 900 °C, this would alter the mechanical properties of the hydrogenated SiC due to hydrogen loss in the film. Also, the film might not be able to sustain the 75 min. buffered HF sacrificial layer etching process. This concern was raised by Dr. Rakhimov who deposits these films.

Sputtered BN is a better candidate, since it is deposited at a much lower temperature of 450 °C. To investigate turn-on voltage lowering of the DVIR tips, 50 µm of BN was sputter deposited by Prof. Pryor. Figure 44 shows the emission current versus gate voltage dependency of a 16 x 16 array, device #1 (3840 tips) with no BN and of a 16 x 16 array, device #62 (3072 tips) with BN and of the same BN coated device #62 after a 10 min. etch in buffered HF.

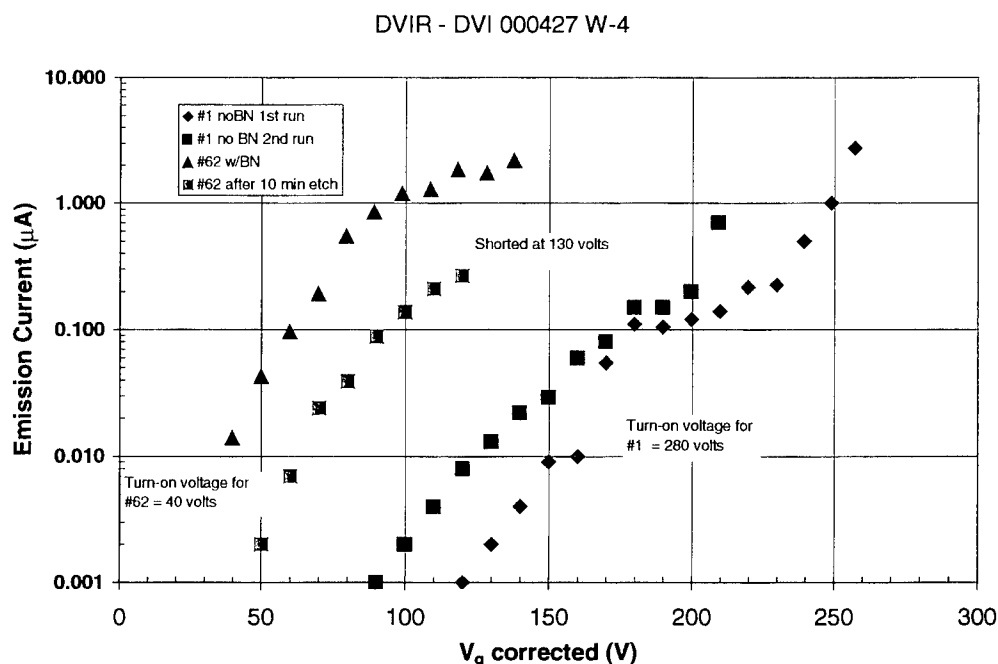


Figure 44. I-V characteristics of a 16 x 16 DVIR array without BN (device #1) and of a BN coated 16 x 16 array (device #62).

Not shown in the Figure is the fact that device # 1 (no BN) had to be biased to 280 V to obtain initial emission. After that, it turned on at about 90-120 V. This is marked as 1st and 2nd run in the Figure. The BN coated device #62 turned on at about 40 V. No high voltage initiation is needed! After a 10 min. etch in buffered HF, the turn-on voltage (which is defined as the gate

voltage to reach 10 nA) increased to about 60 V. We did not investigate the effect of longer etch time or if a low temperature anneal (~150 °C) would possibly restore the 40 V turn-on voltage.

4.5 Vacuum Encapsulation

DVIR devices have to be encapsulated similar to field emitter displays (FEDs). State-of-the-art encapsulation techniques are summarized in [14]. The necessary pressure has to be 10^{-7} Torr or lower. For FEDs, 450 °C frit sealing is acceptable. Degradation in turn-on voltages take place when frit sealing is performed in air. This is caused by additional oxidation of the emitter tips. Sealing at elevated temperatures in an inert atmosphere such as N₂, Ar, with or without small amounts of H₂ prevents degradation. DVIR devices cannot be sealed at 450 °C since pull-in and stiction occurs at those high temperatures. Figure 10 shows the cross-section of the packaged device. After the DVIR chips are mounted and wirebonded, final encapsulation is performed at room temperature using Torrseal.

Prior to this operation, we investigated potential degradation effects upon the field emitter arrays after mounting them to the ceramic substrate and attachment of the gate and shield wires using a polyimide-based silver epoxy (Ablebond 71-1, to be cured for one half hour at 150 °C and one half hour at 275 °C).

Figure 45 shows one example. A field emitter array (6460 tips) was tested prior to silver epoxy bonding. The solid square symbols denote I_{\max} and I_{\min} values of the emission current. The chip was then mounted to the DVIR ceramic substrate with Ablebond 71-1 and some epoxy dots were placed on the contact pads on top of the chips thus simulating the wirebonding operation. After appropriate curing, the substrate/chip was retested in the high vacuum test station. The triangular symbols denote the current values after the bonding procedure. A 20 V shift in the gate voltage is observed, indicating that the tip surfaces were contaminated during the bonding operation.

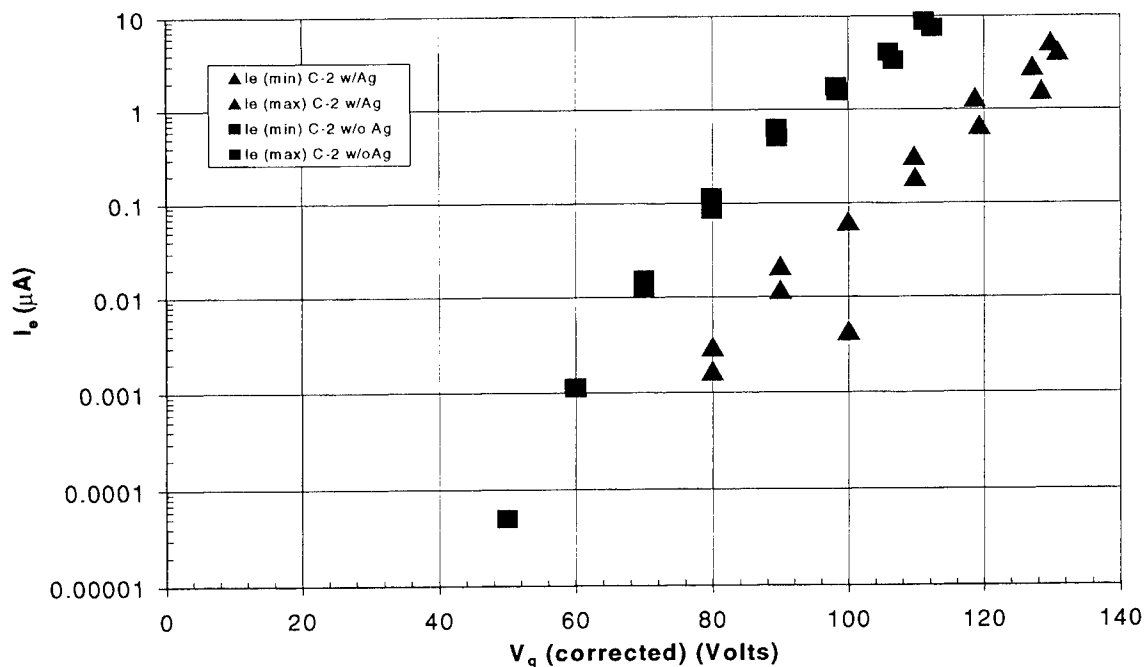


Figure 45. Degradation of the emission current-gate voltage dependence of a 6460 silicon tip array using a polyimide-based silver epoxy (Ablebond 71-1).

The prototypes shown in Figure 1 were encapsulated using the Torrseal method. Figures 46 and 47 show the pin diagrams of Prototype #1 and #2. Prototype #1 contains one DVI 000307 chip and one field emitter array chip that was coated with 10 nm of NCG. Prototype #2 contains one DVI 000307 and one DVI 000427 chip. DVI 000307 has the POCl_3 - doped shield and DVI 000427 has the ion implanted shield.

NC = Not Connected
C/S = Cathode/Substrate

Prototype #1

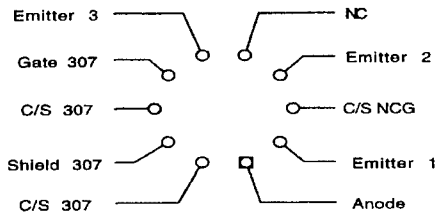
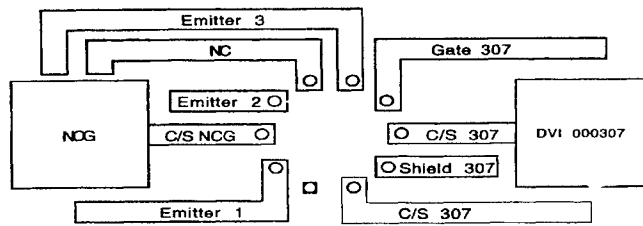


Figure 46. Pin diagram of Prototype #1.

NC = Not Connected
C/S = Cathode/Substrate

Prototype #2

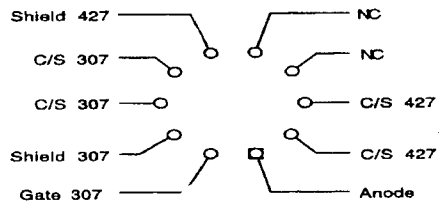
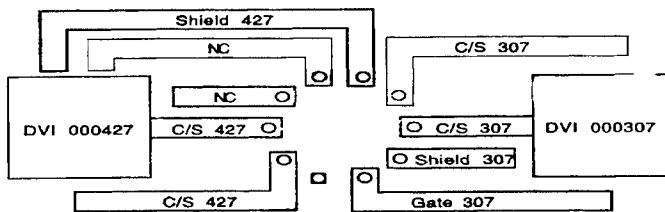


Figure 47. Pin diagram of Prototype #2.

The devices were tested by applying 500 V to the anode. The shield and gate contacts were connected to the gate voltage and the emitter contact was at ground potential. The DVIR chips were fully released prior to encapsulation, as was confirmed by optical profilometer

measurements. It was not possible to confirm if they were still released after vacuum packaging. No emission was obtained to gate voltages of 100 V. At higher gate voltages, flashover events were observed.

The purpose of the NCG coated array was to check if these devices can be packaged without degradation. No emission was observed to gate voltages of 100 V. When the anode voltage was increased to 600 V, flashes occurred. The cause of this failure could be either very poor vacuum, or problems with the anode contact in the package. Thomas Electronics, Wayne, NJ, was the company that packaged these prototypes. Working with Torrseal was new to them. Additional work is needed to develop the appropriate DVIR vacuum package.

5. Conclusions

During this 2-year research effort, we have demonstrated most aspects of the DVIR concept, namely IR activation of cantilever arrays which in turn modulate the emission current of an array of field emitters. Most of the effort concentrated on obtaining field emission prior to cantilever pull-in. To solve this problem, we have developed a MEMS shield technology. By interposing a shield consisting of a thin layer of conductor, a field-free region between the moving MEMS part and the substrate can be obtained if the shield is biased at the same voltage as the MEMS cantilever. We have demonstrated improvements from 2 V to 10 V for flat, leveraged cantilevers, and from 12 V to 30V for curved cantilevers in which the maximum deflection after release was 15 μm for a 110 μm long device (Figure 8).

A major setback in the program occurred when we realized that the shield diameters, which should have been 2, 4, and 6 μm , were actually 6.7, 9.7, and larger than 10 μm . A last lot, in which the shield diameter problem was solved, developed a sacrificial layer problem. No devices could be used from this lot.

Quite a bit of success was obtained in the development of appropriate surface coatings for silicon field emitter tips. These results are applicable for other product uses. It was shown that boron nitride and nanocrystalline graphite can significantly reduce turn-on voltages.

Some work was performed in vacuum encapsulation. It was learned that in order to vacuum package MEMS devices, existing high temperature frit sealing techniques have to be modified.

In summary, we believe that DVIR is a very interesting application for MEMS, but needs quite a bit of additional work to be successful.

6. Recommendations

Some of the recommendations on how to move forward are included in the Overview (Section 1.3.6). These include modeling and optimizing of the shield structure, reducing the turn-on voltages, and the split gate approach.

1. If modeling and improved gate structures reveal that pull-in voltages are limited to the 20-40 V range, then a different tip geometry, other than the Sarnoff tips, has to be used or developed. Prof. Akinwande of MIT [1] obtains turn-on voltages of 15 V. Using his tip technology combined with DVIR MEMS would be one approach to overcome the pull-in problem. We do not know if his tips also need an elevated initiation voltage.
2. The split gate approach that uses the field superposition principle can be developed. By applying most of the gate bias to the stationary portion of the gate (just prior to turn-on) only a small gate bias is needed on the moving MEMS portion of the gate.
3. Noise considerations – For proper performance of the DVIR product, i.e., $NE\Delta T = 100\text{mK}$, the current fluctuations have to be 1% or less per pixel. We have demonstrated that this can be achieved with a 6460 tip array in which the tips are separated by $10\text{ }\mu\text{m}$, the array emission current is $400\text{ }\mu\text{A}$, and the vacuum pressure is about 3×10^{-8} Torr. Current fluctuations increase with pressure and decrease with emission current. An example is shown in Figure 48. It shows $\Delta I/I$ for the above-mentioned silicon tip array, and also for a 100 nm thick NCG emitter that was deposited onto a flat silicon substrate. The extraction electrode diameter for the NCG emitter was about 1.5 mm. What is concluded from that data is that there have to be on the order of at least 1000 emission sites per subpixel. This means that parabolic deflecting cantilevers cannot be used in DVIR, since not all of the emitters experience the same field. Flat plate gate structures that move parallel with the substrate, similar to the device shown in Figure 35 (but with a 10 fold increase in emitter density), have to be developed.

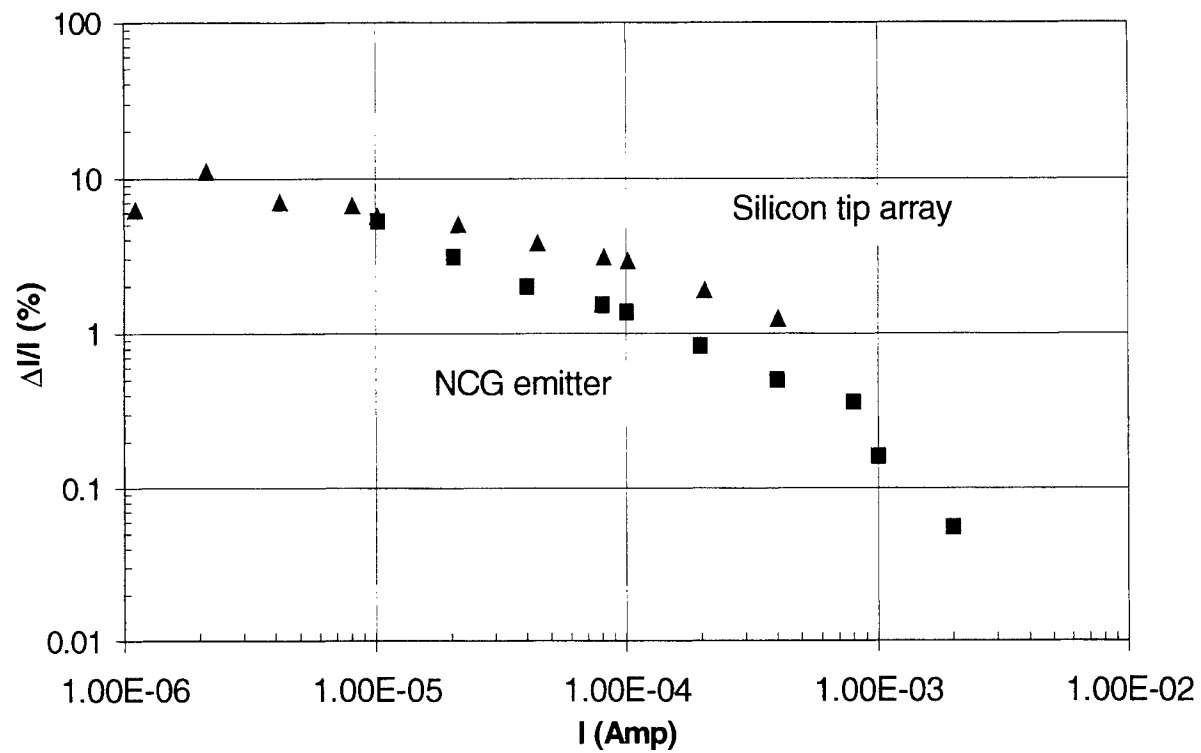


Figure 48. Current fluctuations of a 6460 gated Si tip array and of a 100 nm thick, planar NCG emitter as a function of emission current.

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8. Key Personnel

The following persons were key contributors to this project:

Dr. Frank Pantuso, VP OptoElectronics Business Unit, was the overall leader of this program. Dr. Steve Perna, Group Head, had the managerial responsibility for this program, and Dr. Heinz Busta was the Program Manager. This team was assisted by Dave Furst, who worked on process definition of DVIR and performed all of the lot scheduling and tracking; Dr. Jia Ming Chen, who performed field emitter testing, profilometer measurements, and chip bonding; Dr. Robert Amantea, who was instrumental in shield design and mask pattern development; Steve Rizkowski, who performed most of the field emitter testing and released the structures; and by Don Marinelli, who performed the CO₂ drying operations.

All of the DVIR lots were processed in the Sarnoff IC center. Mr. Michael Della Selva, who is in charge of the IC center showed great interest in this program and pushed for timely delivery. Dr. Larry White performed some of the key processing operations. Prof. Roger Pryor of Wayne State University performed the BN depositions and Dr. S. Rakhimov of Moscow state University performed the NCG depositions.

Appendix A

Description of the First Mask Set

Memo by H. Busta from 12/1/1998

Objective: The objective of this mask set is to fabricate devices demonstrating feasibility of the DVIR approach. This means that field emission modulation can be demonstrated by temperature-activated gates. The mask set will also be used to fabricate devices for stress engineering, for low turn-on voltage field emitters and for determining the lateral thermal resistance of SiC.

The mask set has been designed and four of the nine masks have been ordered. The team consisted of V. Patel, D. Furst, R. Amantea, J. Lawson, V. Frantz, J. Andrews, R. Smeltzer, H. Busta, and F. Pantuso.

In what will follow, some of the devices are marked as SICP, PLAT, and SICP/PLAT. This means SiC coated with a thin film of about 5nm of metal. At present, we plan to use Pt and thus P on the mask set. However, in the future this layer might be replaced by another material such as Cr. PLAT means the thick bimaterial metal which, at present is Pt, and SICP/PLAT means SiC coated with the interconnect layer followed by the bimaterial layer. The SiC is the thermally insulating portion of the bimaterial arm and, in the future, could be replaced by silicon nitride or another material.

The set consists of:

A. Active Devices

A1. Field Emitter Structures without Gate Shields

A1.1. Metal over Half the Arm Length

This is a group of devices with bimaterial arms supporting a gate plate with openings for 1, 5, 10, 20, and 30 emitters. The arm widths are 3, 4, 5, and 6 μ m and the lengths are 40, 60 and 100 μ m. The arms and the gates are fabricated in 0.3 μ m low stress SiC which is coplanar anchored to 0.85 μ m thermal oxide. To provide contact to the gate pad, 5nm of Pt (Cr) will be deposited on top of the SiC. Halfway up the arm from the anchor side, 0.4 μ m Pt (Cr) will be fabricated covering the rest of the arm and the gate plate, except in areas where the emitters are. The width of the Pt is 0.6 μ m less than that of the SiC for the 3, 4, and 5 μ m devices and 1 μ m less for the 6 μ m devices. The hole diameters for the SiC at the emitter tips is 3 μ m, and that of the Pt, which is also the gate diameter is 1.8 μ m.

There are two devices per die for a given group. These devices take up about half the die area and are located on the upper left of the die. There are a total of 120 devices. They are marked with W (width), L (length), and E (# of emitters) letters. Figure A1 shows the perspective view of one of the devices, Figure A2 its cross-section and Figure A3 a top view of a composite consisting of all of the masks.

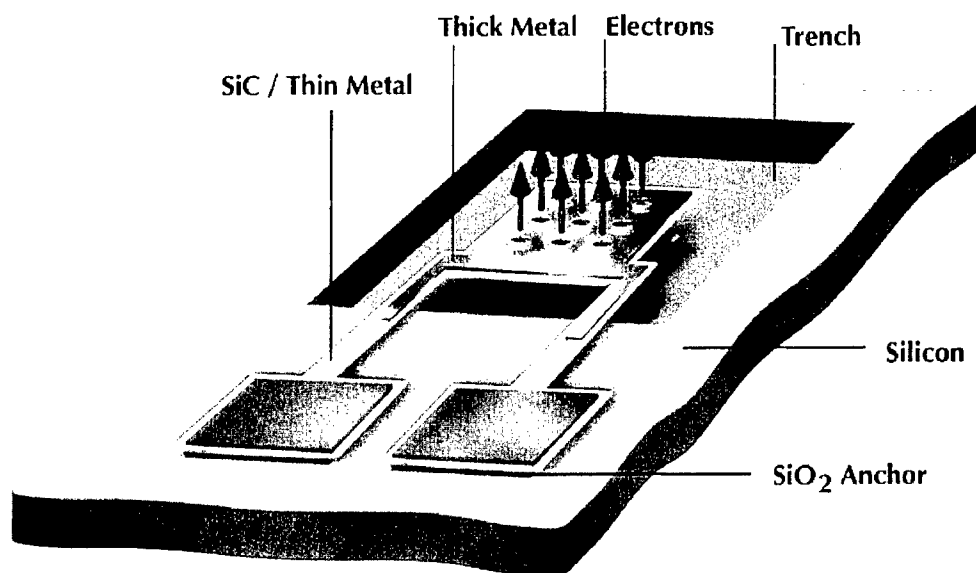


Figure A1. Perspective view of a thermally activated field emitter gate device.

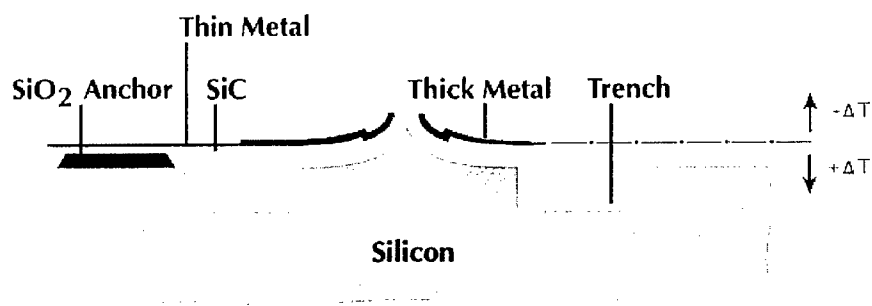


Figure A2. Cross-section of the device in Figure 1.

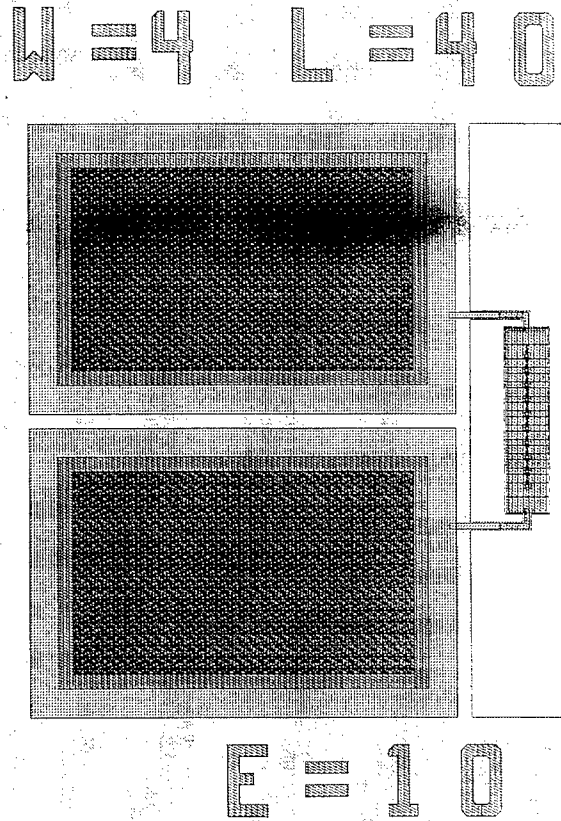


Figure A3. Top view of the mask layout of a $W=4\mu\text{m}$, $L=40\mu\text{m}$ and $E=40$ emitter device.

The thermally insulating and the bimaterial segments of the two cantilever arms as well as the peripheral portion of the gate plate are undercut into a trench to avoid stiction. Dry chemical etching will be used for trench formation. The trench depth is about $10\mu\text{m}$. A layer of photoresist protects the devices during trench etching.

The gates are connected to two pads. By applying probes to both of the pads, the arms can be heated using the thin metal as heating elements. Thus, it is possible to move the gates via the bimaterial arms without applying IR radiation or external heating. This feature will be used in the initial stages of the project to prove feasibility of the concept. Continuity of conduction of the thin metal layer can also be checked by using the two pads.

A1.2. Metal over the Entire Arm Length

Some devices were designed in which the bimaterial metal extends over the entire arm. They were chosen in case that the thin metal is discontinuous, thus preventing electrical contact to the gates. There are 24 devices with $W=4$ and $6\mu\text{m}$, $L=40$, 60 and $100\mu\text{m}$ and with one and five emitters per array. Again, for a given set of dimensions, there are two devices. This group is labeled FULL in the die and is positioned under the 120 'half length' devices.

A2. Field Emitter Structures with Gate Shields

It is expected that the gate voltage pulls the gates towards the silicon substrate, especially at the anticipated gate voltages of about 100V. The magnitude of this effect will be established with the above mentioned group of devices. Even if pull-in occurs, the non-shielded devices can still be used for proof of concept investigation, since the pull-in can be compensated by cooling the devices. However, from a product point of view, it might become necessary to provide a shield between the gate and the substrate. The shield is in close contact to the substrate, but has to be electrically isolated from it since it is biased at the gate voltage, thus creating a field-free region. The insulator upon which the shield is fabricated cannot be removed during sacrificial layer etching and it has to have good insulating properties to support the gate voltage without dielectric breakdown. Another product strategy is to fabricate field emitters that can be operated at about 5-10V to avoid pull-in. This question will be addressed below.

Figure A4 shows the cross-section of a device with the shield and Figure A5 the top view of the mask layout. The shield bias can be applied by the separate contact pad. There are 24 devices on the die with $W=3$ and $5\mu\text{m}$, $L=40$, 60 and $100\mu\text{m}$ and $E=1$ and 10 . Again, two devices per given geometry are on the die. The group is marked SHIELD and is positioned on the lower left of the die.

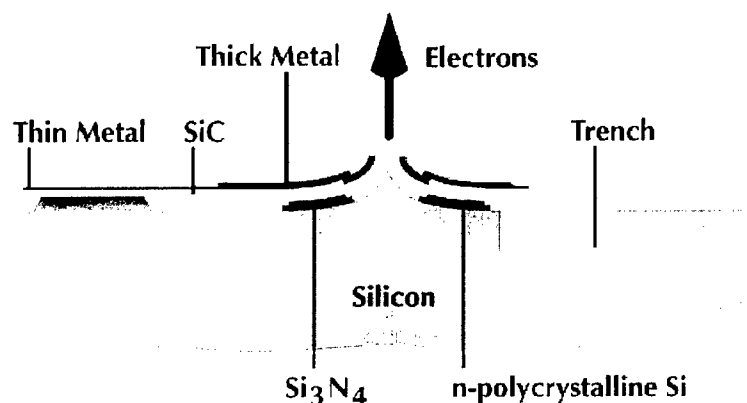


Figure A4. Cross-section of a device with gate bias shield.

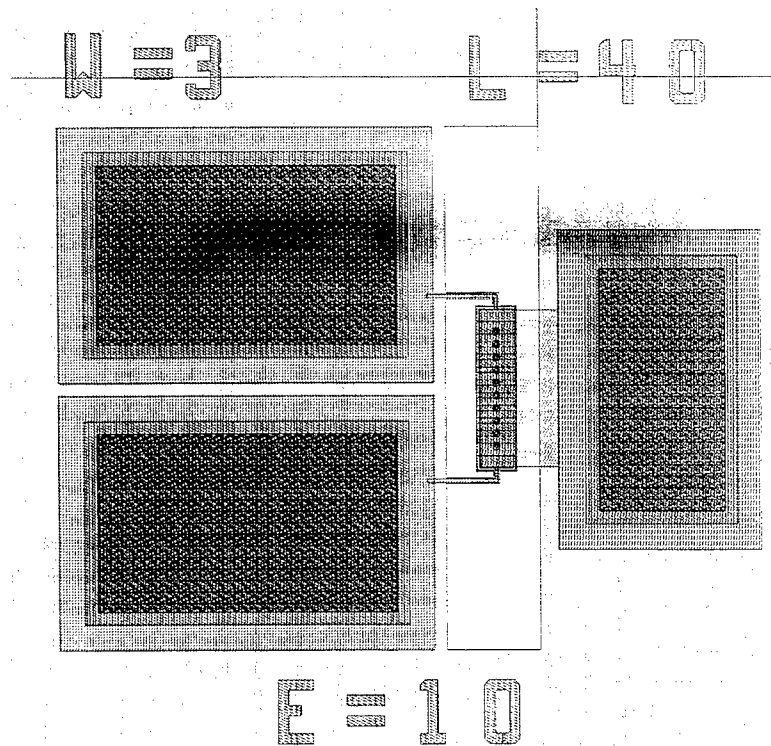


Figure A5. Top view of a device with the gate bias shield with $W=3\mu\text{m}$, $L=40\mu\text{m}$ and $E=10$ emitters.

A3. Four Arm field Emitter Arrays

The devices mentioned so far distort in a parabolic fashion upon heating. This results in nonuniform modulation of the emission current of an $n \times n$ array of emitters, with the largest modulation at the farthest end away from the anchor. To investigate parallel motion of the gate with respect to the substrate, which is the desired case, three test patterns with- and three without shield have been included. The four arms are $100\mu\text{m}$ long, the width of the silicon carbide is $5\mu\text{m}$ and that of the bimaterial metal is $4.4\mu\text{m}$. The emitter array consists of 10×10 emitters which are $10\mu\text{m}$ spaced from each other. The metal extends halfway down the arm. These devices will only work if the arms are under compression. They are located at the lower right of the die and are marked as 4ARM FEA.

A4. Low Turn-on Voltage Field Emitters

For product implementation it is desirable to have low turn-on voltage (5-15V) devices to minimize pull-in and thus eliminate the more complex gate shield process. We have included four devices with 1, 9, 100, and 1000 emitters that are fabricated using a self-aligned technique. In addition, these devices can be fabricated at a much higher density ($2\mu\text{m}$ spacing) versus the $7\mu\text{m}$ minimum spacing of the above devices. This then allows the fabrication of more emitters per pixel resulting in lower noise due to current averaging. Two devices for each set of emitters are on the die and are marked as SELF ALIGNED FEA. The process will be described below.

A5. Schottky Diodes

In addition to gate heating, proof of concept investigation can also be performed by heating the substrate. To be able to measure the substrate temperature directly and not have to assume ideal heat transfer from a heater plate to the wafer in vacuum, a set of Schottky diodes has been included consisting of n-silicon and the bimaterial metal such as Pt or Cr. These diodes will be calibrated by measuring the forward bias at a constant current as a function of temperature. The diodes can also be used as front-side contacts for the pull-in diagnostic structures. The back of the wafer/die is used to provide contact to the emitters. If it becomes necessary to provide front-side ohmic contact, the Schottky device can be used for n^+ implant followed by the metal deposition. If that route is used, temperature sensing cannot be performed on those wafers.

Two of the diodes are placed on the lower right of the die and one near the diagnostic stress patterns. They are marked as DIODES.

A6. Froggy Patterns

Per Frank Pantuso's request, we have included two 'froggy patterns'. The capacitor plates have etch holes at $10\mu\text{m}$ intervals. The bimaterial arms are suspended over trenches to avoid stiction. Two patterns have plate dimensions of $200 \times 300\mu\text{m}$ and two of $40 \times 50\mu\text{m}$. It should be relatively easy to measure capacitance changes as a function of temperature for the two larger patterns.

The patterns serve also a different purpose. As this program matures, it is desirable to fabricate planar emitters which would simplify processing. By using the Froggy pattern after gate hole definition, the oxide can be etched under the holes without releasing the pattern and boron nitride can be deposited into the holes. The top plate is then the gate. Sarnoff, in collaboration with Prof. Roger Pryor is working on this approach. If this approach works, the gate plates can then be released after emitter deposition. Release prior to deposition is not possible since BN is deposited at 450°C . The gates would severely distort at that temperature due to the bimaterial action. The devices are marked as FROGGY and are located in the lower right portion of the die.

B. Diagnostic Devices

There are two groups of diagnostic devices. The first group consists of MIT-developed pull-in patterns and Guckel rings. They will be used for stress, stress gradient, and Young's modulus determination of the cantilever materials. The second group consists of patterns for the determination of the lateral thermal resistance of SiC and SiC/thin metal.

B1. Stress Test Patterns

B1.1 Cantilevers

These patterns consist of beams of bimaterial metal (left group), SiC/thin metal (middle group) and SiC/thin metal/thick metal (right group). The beams are anchored to $0.85\mu\text{m}$ thermal oxide in a planar fashion. They are all $5\mu\text{m}$ wide and are 10, 12, 14, 17, 20, 25, 30, 40, 50, 75, 100 and $200\mu\text{m}$ long. These lengths were determined by R. Smeltzer based on initial calculations and a maximum pull-in voltage of 100V .

By measuring the deflections of the released beams, stress gradients can be determined. By applying bias to the anchor pads with respect to the silicon wafer, pull-in data will be gathered and analyzed.

Some of the 200 μ m beams are processed over trenches except for 20 μ m long portions at the end. By performing pull-in tests, information will be gained about the magnitude of gate voltage that is allowed for negligible pull-in.

All of these beams are marked as PLANARS and are located near the middle on the right side of the die.

A group of SiC/thin metal beams will be fabricated with non-planar anchors. The SiC will be anchored to the silicon through the sacrificial oxide window. The purpose of this pattern is to determine if stress gradients are introduced by the non-planarity. The curvature of those beams will be compared to the curvature of their planar anchored counterparts. These beams are located on the right side of the planar cantilevers and are marked as ANCHORS.

B1.2. Double Anchored Beams (I-beams)

To aid with the stress analysis, double-anchored or I-beams have been included in the mask set. The beams are 5 μ m wide, recessed from the silicon by the thickness of the sacrificial oxide (0.85 μ m), and 20, 30, 40, 50, 60, 80, 100, 120, 150, 200, 300, and 400 μ m long. Three groups consisting of metal (left group), SiC/thin metal (middle), and SiC/thin/thick metal are included. These patterns are positioned below the cantilever beams in the middle right section of the die and are marked as IBEAMS.

B1.3 Guckel Rings

Guckel rings are used to obtain an indication if the films are under tensile stress. A set of trenched rings with outer diameters of 20, 30, 40, 50, 60, 80, 100, 120, 150, 200, 300, and 400 μ m are included. The width of the rings is 5 μ m. The intrinsic tensile stress pulls on the ring portion and causes the inner bar to buckle. For a given stress, bars of a certain length and larger will buckle. The left group of rings is fabricated in SiC/thin Pt, the middle group in thick Pt, and the right group in SiC/thin Pt/thick Pt. The rings are marked as GUCKEL RINGS and are placed on the upper right of the die.

B1.4. Thermal Resistance Test Patterns

The success of this program depends on the thermal isolation properties of SiC. To measure the thermal resistance, six different test patterns are included. They are marked as THERMAL RESISTANCE 1, 2, 3, 4, 5, and 6 and are located below the I-beam stress patterns. Two identical patterns per group will be processed. The patterns consist of trenched SiC arms containing a thin film heater and temperature sensor element. By applying a certain power to the heater, depending on the thermal resistivity of the SiC, it will assume a certain equilibrium temperature. The temperature of the sensing element will also be monitored. From these parameters, the thermal resistance can be calculated. These measurements will be performed in vacuum.

Figures A6-A9 show perspective views of the basic patterns. There are three basic patterns. The first one is shown in Figure A6. The meander-shaped heater/temperature sensor and the

temperature sensor on the far right are fabricated in thin metal and are connected to the thick metal. For all of the patterns $L_s=50\mu\text{m}$, and $L_b=25\mu\text{m}$. $W_b=20\mu\text{m}$ for patterns 2, 3, and 6 and $5\mu\text{m}$ for patterns 4 and 5. For pattern 1 it is $120\mu\text{m}$. Only two W_b sections are shown in Figure A6. The devices 2, 3, and 6 have actually four SiC sections. The isothermal bars shown in Figure A6 are fabricated in thick metal. The pattern shown in Figure A6 is device 6 on the die. Device 3 is identical to device 6 except that the $L_b \times W_b$ rectangles have the thin metal left on top of the SiC. From these two devices, we should get an estimate about the thermal shunting effect of the thin metal interconnect. Device 2 is identical to device 3 except that the thick metal crosses the L_s arm to connect to the meander heater/sensor. This avoids heating of the arms.

Figures A7 and A8 show devices 4 and 5. Here the thermal resistance of $5\mu\text{m}$ wide arms will be measured. The difference is that the thin metal is left on top of the SiC in Figure A7 (device 4) and is removed in Figure A8 (device 5). The difference in data should yield the heat shunting effect of the thin metal similar to devices 3 and 6 for the wider arms.

Figure A9 shows device 1. This is a cantilever structure and does not have a separate temperature sensor.

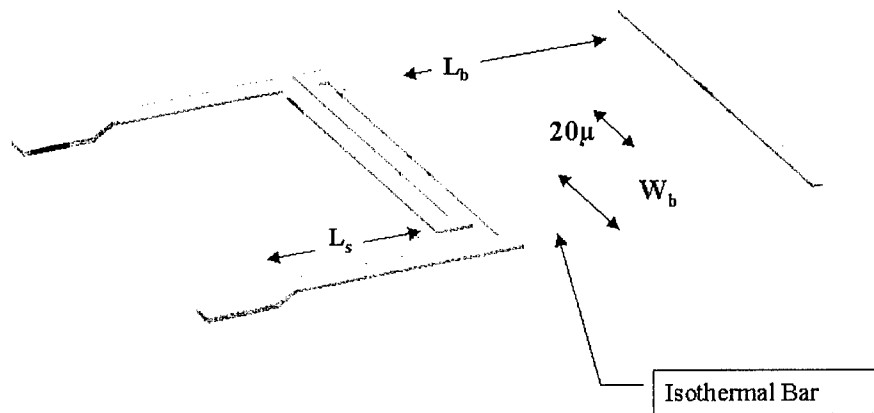


Figure A6

Figure A6. Test patterns for measuring the lateral thermal resistance of SiC and of SiC shunted with a thin layer of interconnect metal.

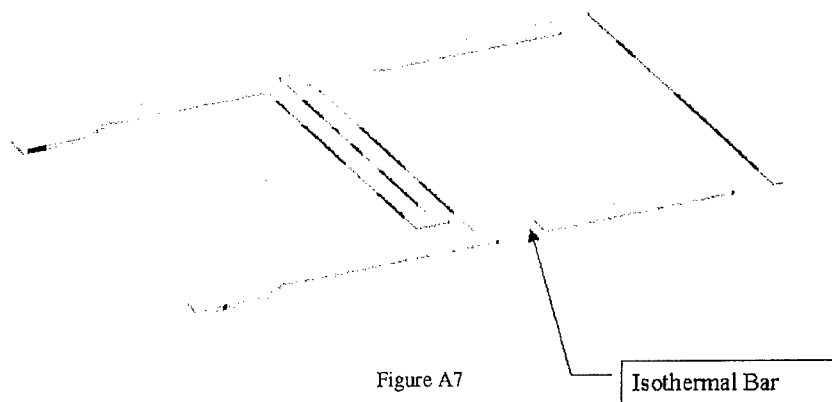


Figure A7. Test patterns for measuring the lateral thermal resistance of SiC and of SiC shunted with a thin layer of interconnect metal.

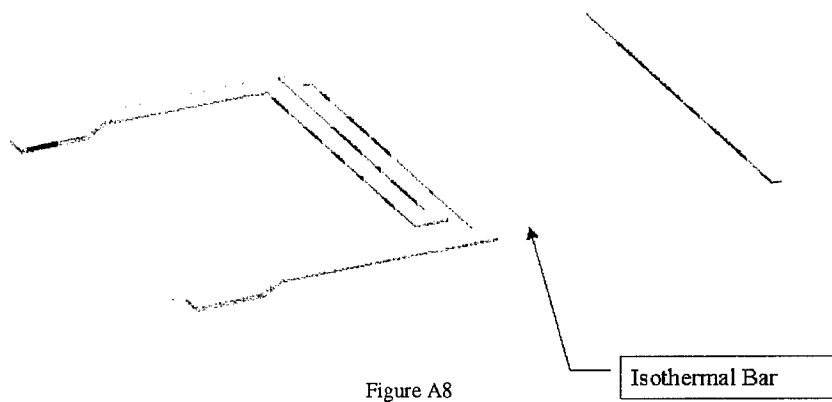


Figure A8. Test patterns for measuring the lateral thermal resistance of SiC and of SiC shunted with a thin layer of interconnect metal.

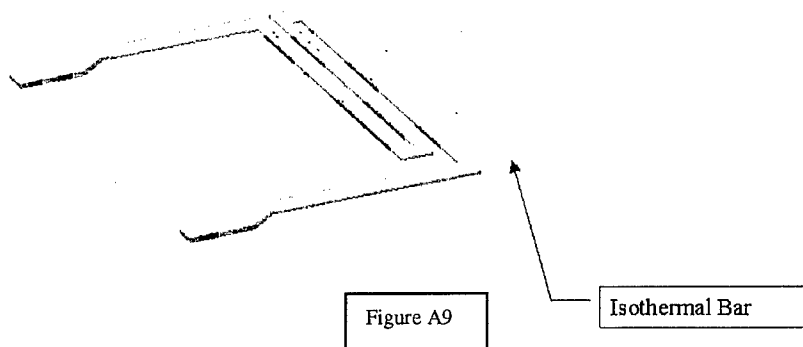


Figure A9. Test patterns for measuring the lateral thermal resistance of SiC and of SiC shunted with a thin layer of interconnect metal.

C. Alignment Keys

In order to align different mask layers using the Canon stepper, Sarnoff has developed its own alignment key methodology. These keys are located under the Guckel ring patterns.

Figure A10 shows the overall layout of the die, designed to demonstrate feasibility of the DVIR approach.

SARNOFF Proprietary

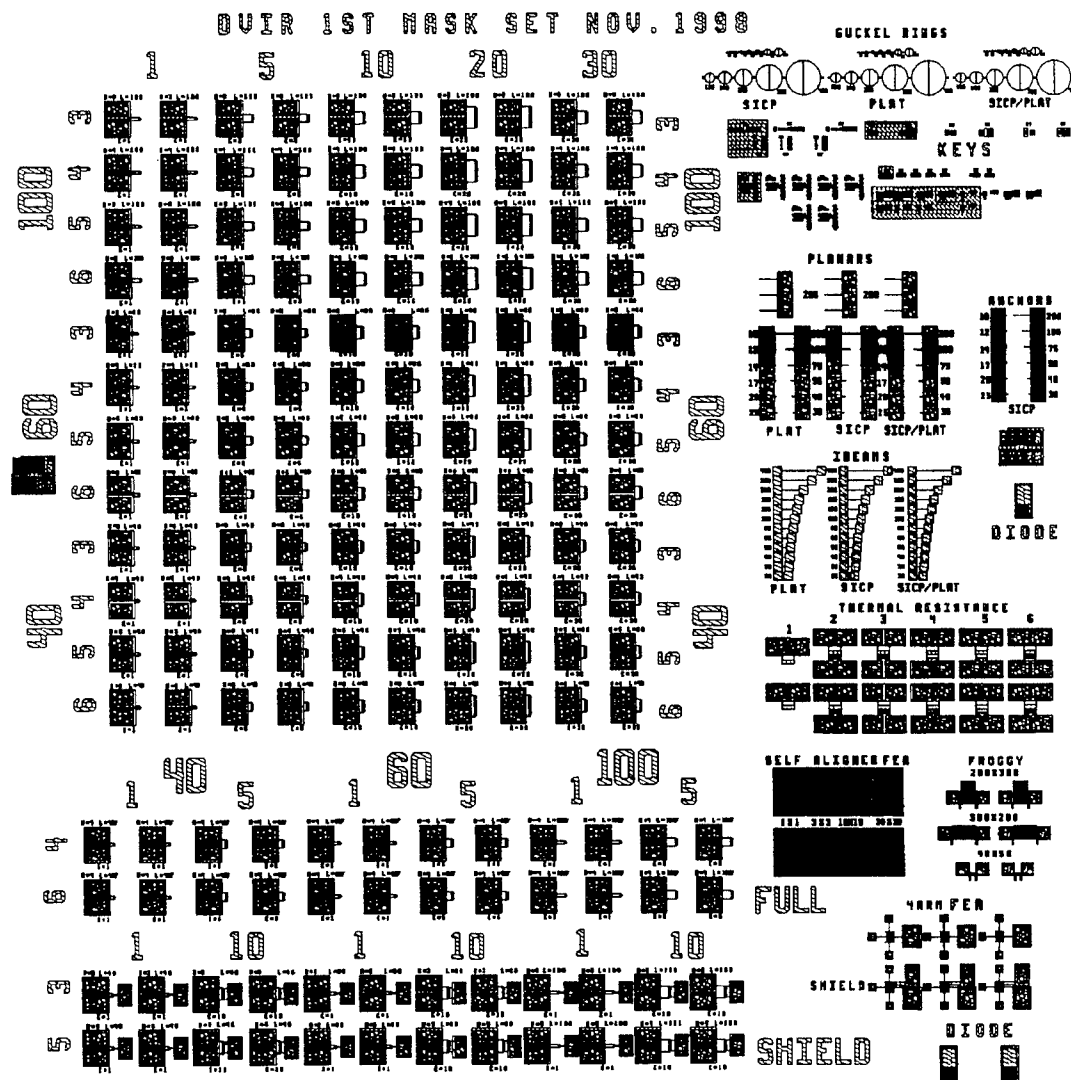


Figure A10. Layout of the test patterns for DVIR proof of concept phase and stress engineering during process development.

Processing

There are nine masks for processing these devices. PR5DVIR01 is the initial key mask. Keys are defined in a layer of 20nm oxide under a 50nm silicon nitride layer. The first mask also contains 1.4 μ m diameter dots for the definition of silicon tips for the self-aligned FEA array. To finish these devices, a separate lot has to be scheduled.

PR5DVIR02 contains, in addition to key protects, the 6 μ m diameter cathode dots that are used in our standard FEA process. These dots are fabricated in photoresist. The mask also contains the gate outline for the self-aligned FEAs. It will be used to remove unwanted gate material between the FEAs.

PR5DVIR03 contains the SiC/thin metal patterns. Both layers will be removed during the dry chemical etching step.

PR5DVIR04 contains all of the thick metal patterns. Thick metal is defined by a lift-off process.

PR5DVIR05 defines the thin metal on top of the SiC and is only used to fabricate the heater, sensor and shunting elements for the lateral thermal resistivity patterns.

PR5DVIR06 is the Al bonding pad mask. This mask will be used if some of the devices will be packaged and wire bonded.

PR5DVIR07 is the trench etching mask. Trench etching is a dry etching process. The maximum trench depth is about 10 μ m.

PR5DVIR08 is the sacrificial oxide window etch mask to define the contact region for the Schottky diodes and the SiC/thin metal cantilevers anchored to the silicon substrate. Some openings are also provided for the self-aligned FEA during etching of the oxide to expose the tips. The oxide at the periphery of the gate is protected by this mask. This avoids peripheral shorts.

PR5DVIR09 is the gate shield mask. At present, we plan to use silicon nitride as the insulator on top of silicon and lightly doped polycrystalline silicon as the gate shield. These two materials will be deposited in sequence and etched in one masking step. The patterns are big enough so that dielectric breakdown of the insulator with respect to silicon can be tested directly using these patterns. SiC can also be used instead of the silicon nitride. Electrical integrity of the SiC can be tested by using the anchored SiC pattern prior to sacrificial oxide etching so that the cantilevers cannot pull-in and short to the substrate.

Initial Processing Strategy

Device processing will take place in several stages. Initially, active devices will be processed without the gate shield. This is followed by processing of the thermal resistance pattern and by processing of devices with the gate shield.

Active devices without gate shield

Mask DVIR01	Si ₃ N ₄ (250nm)/SiO ₂ (36nm) keys
Mask DVIR02	6µm diameter photoresist dots Partial etching of tips Remove photoresist Oxide sharpening, 0.85µm oxide
Mask DVIR08	Define oxide window for diodes and anchored beams Etch oxide, strip resist Deposit 0.3µm SiC and 0.005µm Pt(Cr)
Mask DVIR03	Etch SiC/thin Pt to form gates and arms Strip resist
Mask DVIR04	Define thick metal patterns with photoresist Deposit 0.4µm Pt Lift-off photoresist
Mask DVIR07	Deposit resist, define trenches Dry etch trenches, 10-12µm deep Remove resist Release in buffered HF Test

Thermal Resistance Pattern

To process the thermal resistance pattern, the process described above is used up to the SiC etching, Mask DVIR03. At that point, the thin metal layer has to be defined to form the heating/sensing elements. This is done with mask DVIR05. After that, the process as outlined above is continued.

Self-aligned FEA

The first mask is used to define 1.4µm diameter dots of SiO₂/Si₃N₄. This is followed by isotropic tip etching, leaving a small plateau of silicon at the SiO₂/Si₃N₄ interface. This is followed by tip sharpening by forming a 0.5 - 0.85µm thick oxide. This is followed by e-beam deposition of the gate metal and etching of the gate periphery using mask DVIR02. Next, Al is deposited and photoshaped using mask DVIR06. This is followed by depositing photoresist and using mask DVIR08 to define a window exposing the tip regions of the arrays. This is followed by buffered HF etching to lift-off the Si₃N₄ caps and to remove the oxide near the tips. After photoresist stripping, the devices are ready for testing.

Appendix B: Examples from the Second Mask Set

Two representative examples of patterns from the second mask set follow.

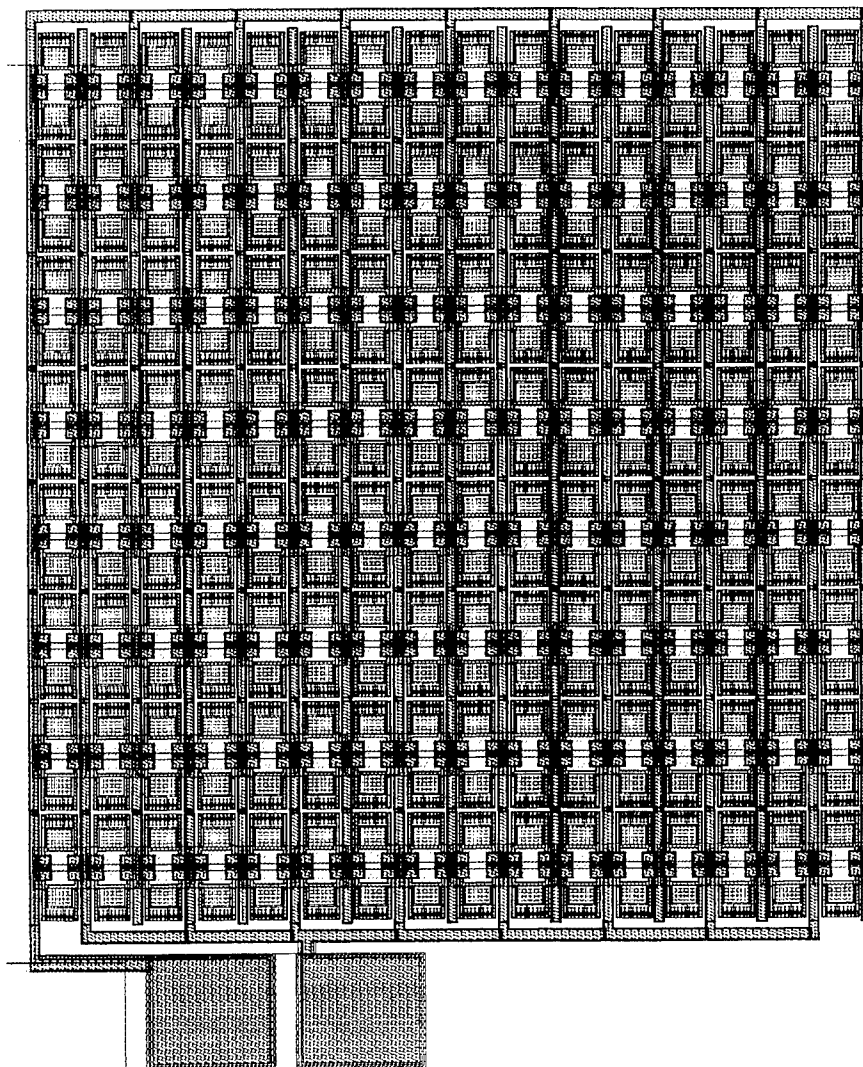


Figure B1. Top view of the 16 x 16 DVIR array that is described in Figures 2 and 40.

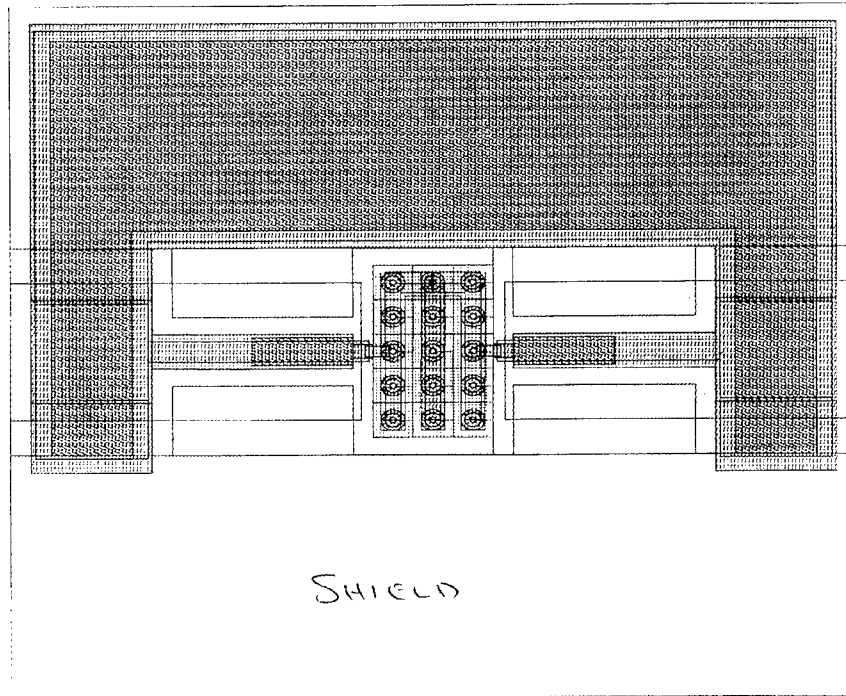


Figure B2. Top view of a 15 emitter device in which the gate plate moves parallel to the substrate. For DVIR to be successful, this type of device has to be used over the parabolic deflecting devices.

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